CHAPTER-V

ELECTRONICS OF THE RECORDING SYSTEM AND RESPONSE - CALIBRATION

5.1 Introduction

The pulse height recording system for a large number of channels from scintillation counter of an air shower array is designed and assembled by the North Bengal University Air shower group[1,7,10,12]. Analogue pulses from the array of detectors carrying particle density information is received by the pulse height recording system. This recording system contain selection system unit, Master control unit, sample and Hold Unit, Clock pulse Unit, Analogue to Digital Converter (ADC), ADC programme unit, Analogue Multiplexer and Demultiplexer, Display unit, Memory, Memory programme unit and last of all printer. The selection system is controlled by the Master control unit which controls the operation of the whole circuit and the digital output of the analogue pulse is printed on a paper tape by means of a line printer. The block diagram of the circuit is shown in fig. 4.7 (Chapter-IV). The coincidence master pulse is used to trigger the flash tube chamber control unit and the magnetic spectrograph control unit.

All the scintillation detectors are calibrated for single particle pulse height with G.M. telescope and the efficiency of each of the detectors is measured. The response of the flash tube chamber is tested by means of G.M.telescope for different position of the flash tube chamber.

5.2 Description of the electronic circuit and its operation

In the present form of array (fig. 4.1 Chapter-IV) there are 16 scintillation counters. The output of each scintillator is amplified by preamplifier of gain 30 using operational amplifier 531. The output pulse of each preamplifier is conveyed to recording system (fig. 4.7) by RG11U coaxial cable. These output pulse from preamplifiers are further amplified of gain 10 by means of operational amplifier having an analogue switch at the input. The outputs from amplifiers are fed to the "Sample and Hold" circuits. The "Sample and Hold" unit retains the peak of analogue pulse for about 3 μs during sampling and fed to the ADC for scanning through Analogue multiplexer if there is hold command from the master control unit. In the selection system, any three adjacent scintillators in triangular symmetry with central one as common are taken to produce a coincidence pulse to trigger the (1) Master Control Unit, (2) Flash tube chamber control unit and (3) Magnetic spectrograph unit. As soon as the master control unit is triggered it gives a hold command to the 'Sample and Hold' unit, switches off the input line of the amplifier, disconnects the coincidence circuit from the master control unit and sends a start pulse to the programmed ADC and memory programme unit. The neon tube glow information of the magnetic spectrograph received at data latch is stored by the master control unit in a separate memory. The-built-in-programme unit controlling the ADC, once triggered, connects the 1st channel of the 'Sample and Hold' unit through analogue multiplexer and digital display system through digital demultiplexer to the ADC; at the same time it resets the ADC output counters connected to the memory. At the end of these operations it gives a start pulse to the ADC. At the end of ADC conversion the ADC programme gives a write instruction to the memory programme

unit which writes the data in the memory and advances the memory channel by unity. ADC programmer then connects the 2nd channel of the "Sample and Hold" unit and the digital demultiplexer to the ADC for scanning. The operation is repeated for all the 16 channels at the end of which ADC programmer gives a 'print in black' command to the line printer through memory programmer resetting the memory address register. The hold command to the 'Sample and Hold' unit from master control unit is withdrawn after the ADC scan. The blanking input to the digital display system is withdrawn for a certain interval of time so that one can visually check on the digital output from the ADC. The master control unit then resets all the counters of the display system. The memory programmer gives the printing instruction for all the 16 channels at the end of which it connects the line printer to the digital information of neon tube glow of the magnetic spectrograph. All the tube information are printed in octal system discussed latter (in section 5.10). At the end of printing, the analogue switches are switched on and the coincidence circuit is gated on to the master control unit for the next event. The output from the preamplifier is scanned to see whether there is any saturation at the output of the amplifier which will occur for large signal at the input. Since the preamplifier is of gain 30 the maximum voltage that can be recorded by scanning the preamplifier output by means of the ADC is 300 mv at the input point.

5.3 Selection system and coincidence unit

The circuit that controls the system of selecting the scintillator pulse to produce a coincidence master pulse for the detection of arrival of air shower is termed as the selection system and coincidence unit and is shown in fig. (5.1). The output of each scintillator is representing a

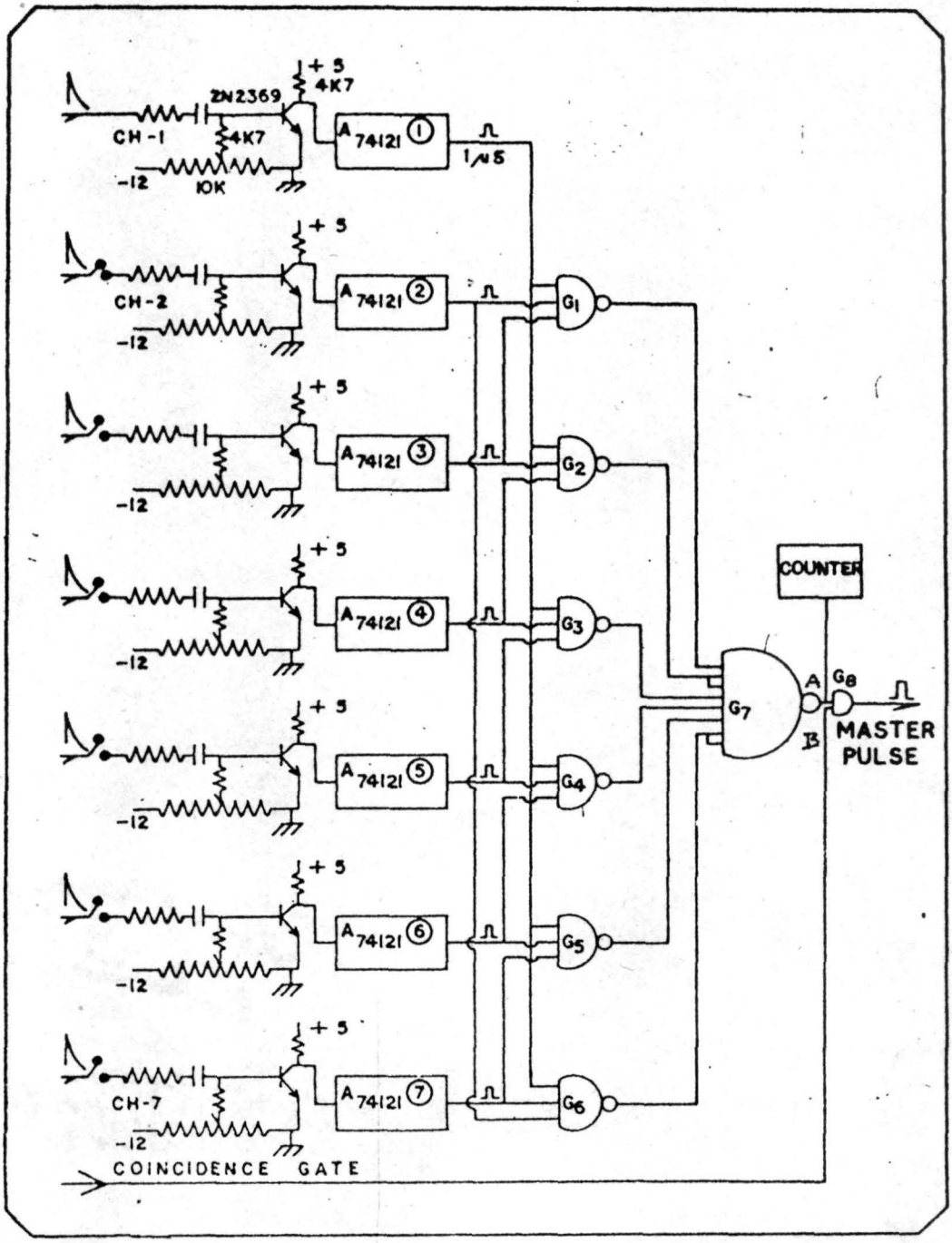

FIG. 5.1. SELECTION SYSTEM AND COINCIDENCE CIRCUIT.

channel. In the present form of experiments, seven channel (1 to 7) are taken in the selection system. First channel is representing the central scintillation counter and other six are in hexagonal form around first scintillator. The output of the last stage amplifier may go upto 10 volts from 7 channels and are fed to 7 switching transister (2N2369) of variable bias through 'ON' 'OFF' switches. The output of these switching transistors are used to trigger 7 monostable multivibrators (IC-1 to IC 7 in fig. 5.1) to produce 1.5 /us pulse width. Out of 7 channels any three of them are in triangular symmetry with 1st channel as common in the central region. The 1.5 /us width pulse of the multivibrators are fed to 3 input NAND gate G_1 to G_6 which produces coincidence pulse by the combination of 7 channels with 1st channel as common (fig. 5.1). With hexagonal configuration the maximum number of such triggering is six. The output of all gates (G_1 to G_6) are fed to the 8 input NAND gate G_7 which is operated in negative logic. Thus the presence of coincidence pulse in any one of the gate (G_1 to G_6) produces a positive pulse at the output of G_7. By adjusting the bias of the transistor (2N2369) we can demand high particle density at the detectors which are situated in the hexagonal region of the array (i.e., array centre). The output of G_7 is fed to the two input AND gate G_8, one of the input (A) of which acts as a coincidence gate and other input (B) is kept normally high by means of master control unit. The output pulse of G_8 is taken as the master pulse. This master pulse trigger the master control unit which inturn makes low one of the input (B) of gate G_8 which was previously in high state. By this procedure G_8 stops the

further generation of master pulse. At the end of whole operation of the recording system, the input B of G_3 is made high by means of master control unit for the next event to record. The output of G_7 is also connected to a counter to record coincidence rate. The width of the pulse shaped at monostable multivibrator is 1.5 /us and the chance coincidence is observed less than 2% for three fold coincidence.

5.4 Control Unit and High Voltage Unit of Flash Tube Chamber and Magnetic Spectrograph

The fig. (5.2) and (5.3) representing Control Unit and High Voltage pulsing unit of Flash Tube Chamber and Magnetic Spectrograph Units. The master pulse from the selection system is fed to trigger the first thyratron 2050 (fig. 5.2) to operate two relays, one for camera and other for fiducial lamp of the Flash tube chamber and Magnetic Spectrograph Unit. The output pulse from first thyratron fig. (5.2) fires a second thyratron fig. (5.3) which in turn discharge a condenser (0.05/uF) charged to + 12 KV through 100 Ω noninductive resister. The resulting high voltage pulse is applied to the electrode plates between the layers of flash tubes. The first relay is used for winding the film in the camera which records the glow information of the event photographically and also for paralysing the first thyratron (2050) for a certain interval of time.

5.5 Master Control Unit

The master control unit is the main unit which controls the operation of the different parts of the recording system. This unit is triggered by the master pulse. The diagram of the

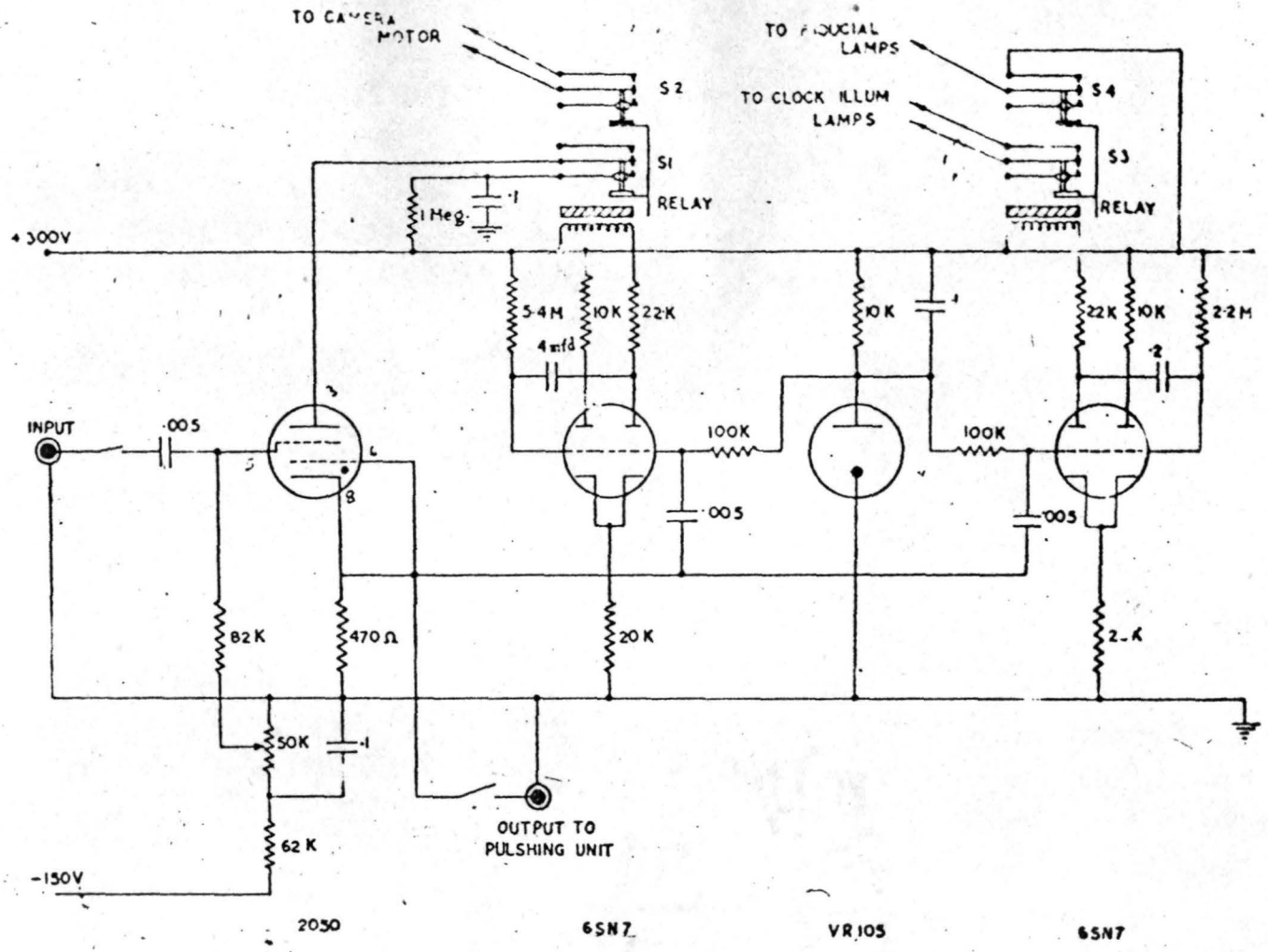

FIG. 5·2 MAGNETIC SPECTROGRAPH AND FLASH CHAMBER CONTROL UNIT

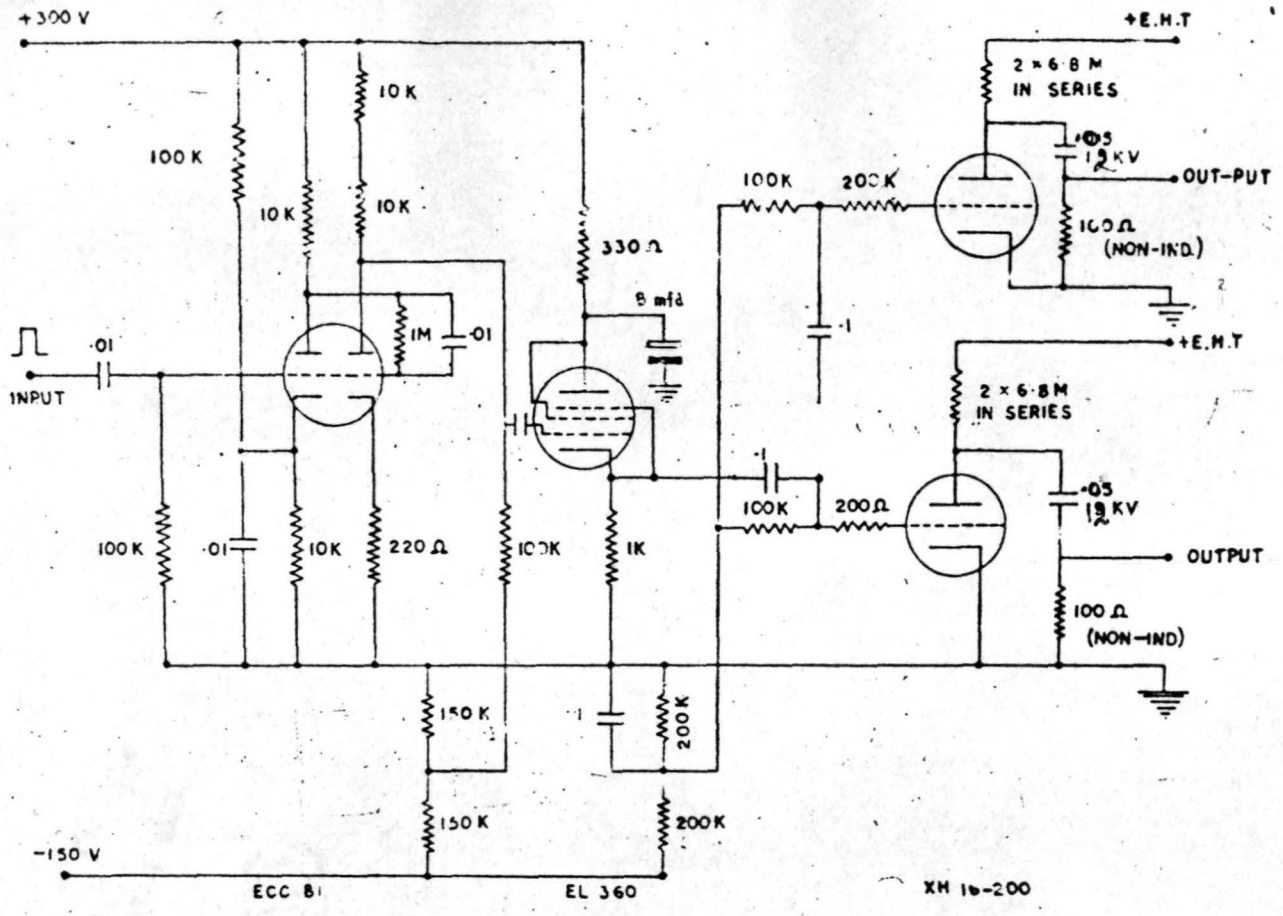

FIG. 5.3 MAGNETIC SPECTROGRAPH AND FLASH CHAMBER HIGH VOLTAGE PULSING UNIT.

master control unit is shown in fig. (5.4).

As soon as the master pulse is generated it triggers monostable multivibrator IC1 and IC2. IC1 produces the start pulse which gives the execution command to the ADC programmer and memory programmer and write pulse to the memory of the magnetic spectrograph memory unit. IC2 gives a hold command to 'Sample and Hold' unit to hold the peak of the analogue pulse. IC5 is triggered at the end of master pulse to operate the set-reset latch R/S to close the coincidence gate and open by the reset counter (IC-6) by making 'Reset to Zero' (R_o) input low.

After triggering the master control unit by master pulse a definite time is required to measure the pulse height and to print all the information on a paper tape. This time is adjusted by means of a preset counter IC6. The preset counter is so adjusted that at the end of the print the preset counter, operating set-reset latch (R/S), makes the coincidence gate B of G_3, fig. 5.1) and 'reset to zero' input of the preset counter high for the next event to record.

At the end of the hold command to the 'Sample and Hold' unit, IC3 is triggered to produce a display pulse. This display pulse is used to display the digital output of ADC for visual check. At the end of display pulse IC4 is triggered to reset the digital output of the ADC to the display unit.

The width of the hold command is greater than the time required for analysis by the ADC and the width of the display pulse is about 0.5 sec. for convenience of visual check. The width of the start pulse is greater than the voltage setting time of the

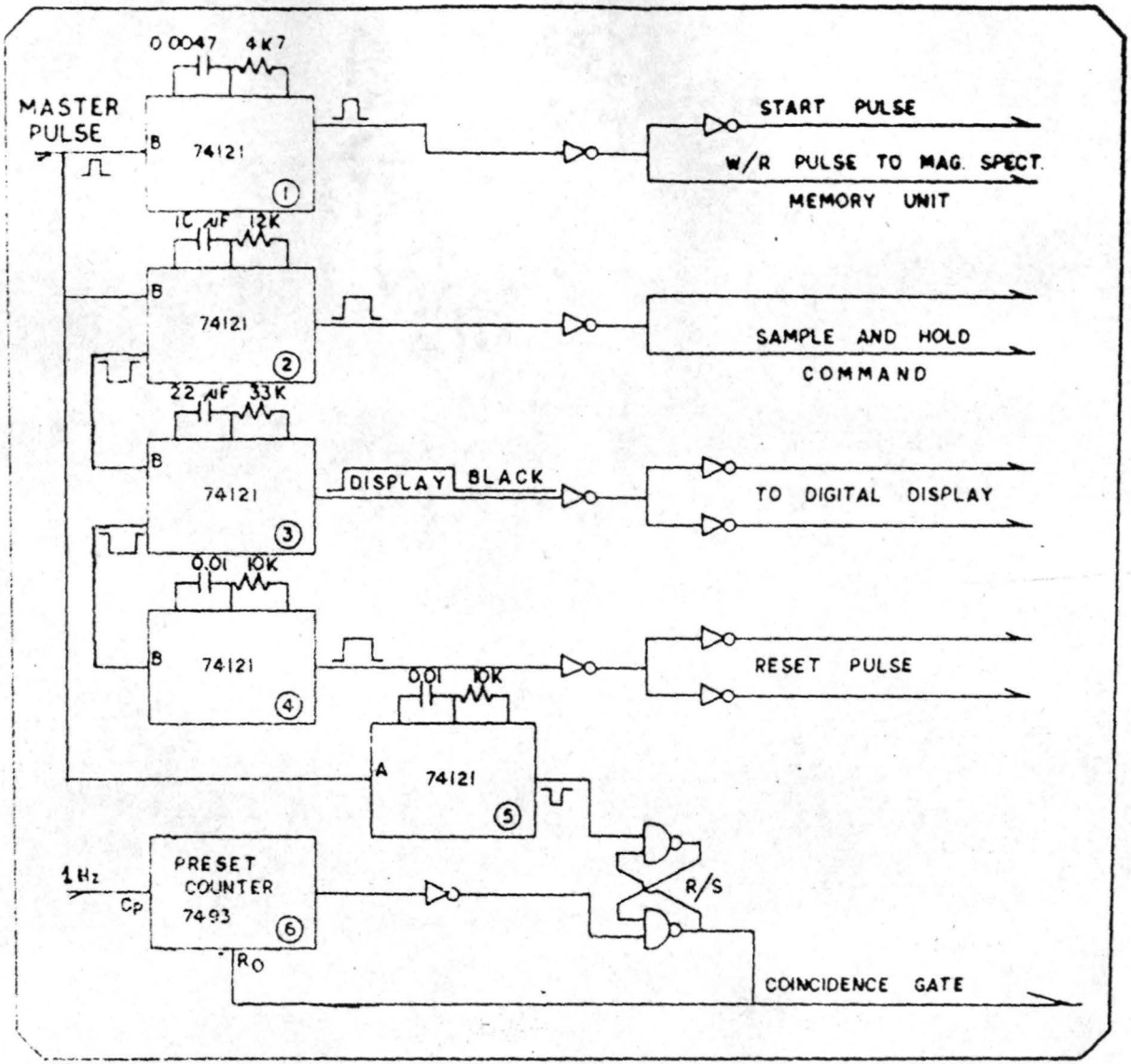

FIG 5.4 MASTER CONTROL UNIT.

analogue multiplexer.

5.6 'Sample-Hold' and Analogue multiplexer for multidetector system

The 'Sample and Hold' and analogue multiplexer system can be realised in various ways (Ref. 2-6). The basic principle of all circuits is same. The detection of peak, monitoring during sampling, holding the peak of a selected pulse and then feed it to the ADC through analogue multiplexer are simultaneously made by means of a simple circuit (Ref.7) which were not provided previously. The new form of circuit is always adjustable both for holding time of the peak during sampling and closing the input line after a definite time of interval or instantaneously. Realisation of analogue multiplexer is made simply by FET switches operated by operational amplifier and TTL ICs.

5.61 Principle of Operation

Charging a storage capacitor upto a voltage equal to the peak of the analogue pulse by means of a conventional peak detector used in almost all cases of analogues peak detection in analogue systems, is utilised in the working principle of the sample and hold circuit. The voltage across the capacitor is retained for a few microseconds and then allowed to discharge through a switch for sampling. A 'Hold command' cuts off the discharging path of the capacitor and the input line. The 'Hold' command further connects the analogue multiplexer consisting of FET switches and operated by logic pulses to the output of sample-and-hold units for scanning with an ADC.

5.6.2 Description of the circuit

The circuit diagram for the system is shown in fig. (5.5). The whole circuit is composed of two parts :

(1) Sample and Hold (S-H) consisting operational amplifiers (op.amp. IC-1 to IC3), TTL Ic's (IC-6 and IC7), two field effect transistors (FET) T_1 and T_3 and a silicon transistor T_2 for each channel together with an operational amplifier (IC-4) and TTL IC's (IC-8 and IC-9) for general control of all the input lines.

(2) Analogue multiplexer consisting of TTL IC's (IC-10, IC-11) for channel address and decoding and an op.amp. (IC-5) together with a FET (T_4) and a diode to switch 'ON' and 'OFF' for each channel.

For each channel the analogue pulse is fed to a peak detector unit consisting of an op.amp. (IC-1), a diode and a capacitor C and to the base of the transistor T_2 through 10 kΩ resistor. The drain of T_1, acting as an input switch, is connected to the input line. Transistor T_2, acting as a logic level Clipper is to operate IC-6 with the input pulse. Transistor T_3 operated by IC-3 acts as a switch to discharge the capacitor C by triggering IC-7 after a definite time from the arrival of a pulse controlled by pulse width of IC-6. The triggering of IC-7 is controlled by connecting the 'S-H Command' to the reset input. The output of the S-H unit is taken by a voltage follower (IC-2).

The drain of the transistor T_4 acting as the first

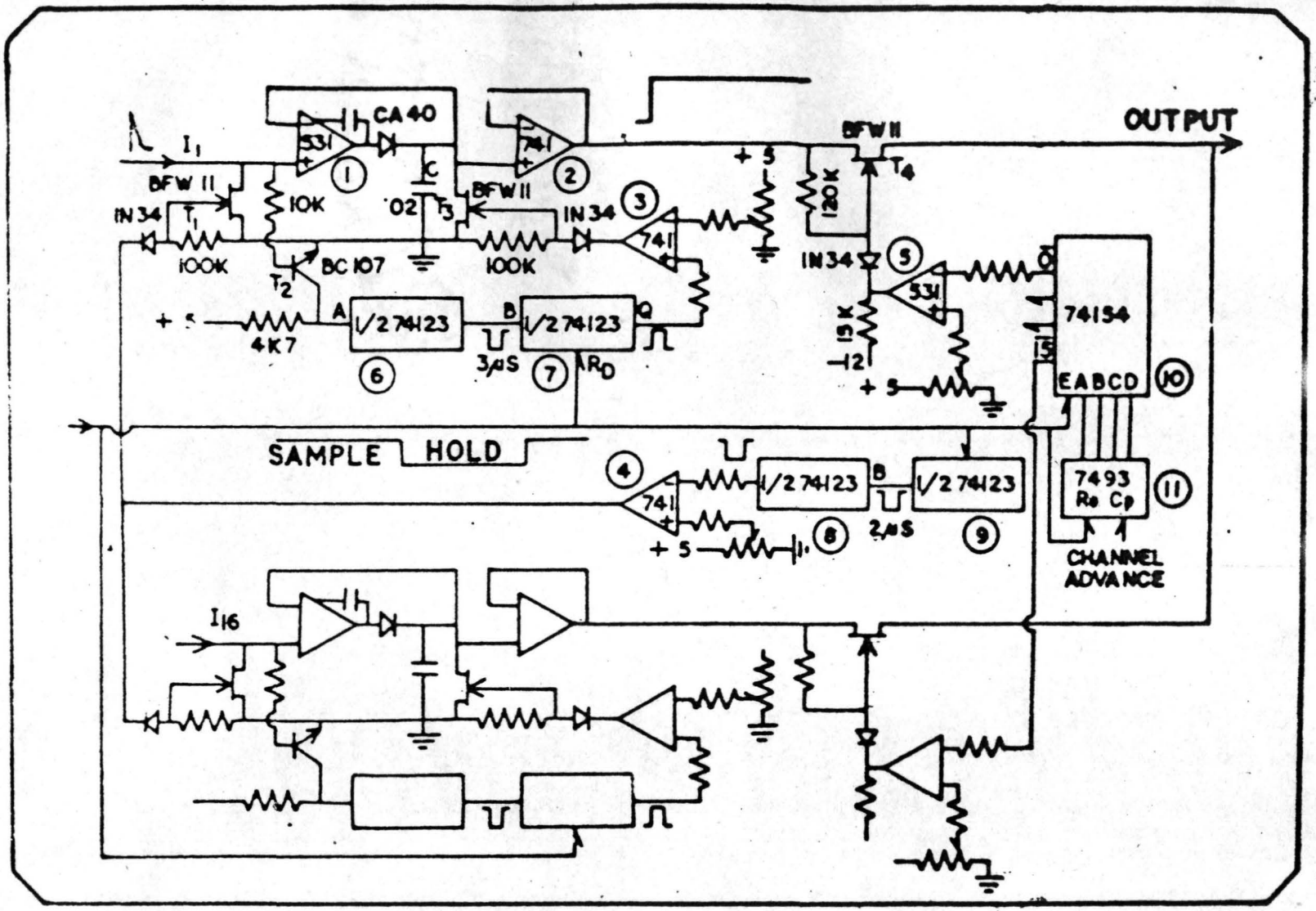

FIG. 5.5 CIRCUIT DIAGRAM OF SAMPLE-AND-HOLD AND ANALOGUE MULTIPLEXER UNIT

channel input of the analogue multiplexer unit is connected to the output of the S-H unit and to the gate of T_4 by 120kΩ resistor. The gate is connected to the output of a high slow rate op.amp. (IC-5) through a forward diode. A small voltage, about 1 volt, is applied to the non inverting input so that when the output of IC-10 is low the gate of T_4 goes to drain voltage and when the output is high the gate goes beyond the drain current cut off value switching off the input-output line. All the source terminals of the FET switches operating in the position T_4 for 16 channels are connected together to give the output. Sequential connection of the channels is obtained by decoding channel address with IC-10 generated by IC-11 which contains a channel advance instruction at the C_p input. R_D of IC-7, enable control (E) of IC-10 and R_0 of IC-11 are held high during sampling and low on giving a 'hold command' which closes the input line after 2 μs by operating IC-4 which makes the transistor T_2 conducting. The $\bar{Q}$ output of IC-6 of all the channels is multiplexed and connected to 7 segment LED display for monitoring (shown in fig. 5.6).

5.63 Operation of the circuit

Analogue pulses to be analysed coming from 16 detecting units are applied to the inputs I_1 to I_{16}. Any analogue pulse at input I_1 (say) will charge the capacitor C at a voltage equal to the peak of the analogue pulse by means of high speed op.amp. IC-1 acting as a peak detector and is measured by the voltage follower IC-2. The drain current of transistor T_3 is normally cut off. The input pulse triggers IC-6 through transistor T_2 which produces a 3 μs width pulse. At the end of 3μs, IC-7 is triggered to

discharge the capacitor C by making the transistor T_3 conducting. Thus the peak of each pulse is held for 3 /us during sampling. As the 'Sample and Hold' input is held high during sampling 'enable control' (E) of IC-10 and R_D of IC-11 are also high so that IC-11 is at zero address and all the outputs from the decoder (IC-10) are high. Thus all the outputs from S-H are cut off by FET switches operating in the position T_4.

The Control Unit of the detector array contains TTL logic gates. The generation of 'hold command' is almost instantaneous with the arrival of the selected pulse and hence falls within the sampling time of 3 /us. The 'hold command' makes R_D of IC-7, E of IC-10 and R_D of IC-11 low; at the same time it triggers IC-9 to produce 2 /us width pulse. At the end of 2 /us, IC-3 is triggered to close all the input lines by making the input controlling transistor, in the position T_1, conducting. The width of the pulse from IC-3 must be greater than the time required for analysis. The input line is closed after 2 /us from the 'hold command' to ensure full peak value at the peak detector stage though it is operated by a fast operational amplifier. As R_D of IC-7 is low it will not trigger and the voltage across the capacitor C is retained. The wave-form of the pulse after a 'hold command' is shown at the output of IC-2. The hold command connects the first channel to the output by making the output O of IC-10 low and counter (IC-11) ready for addressing the channels. All the 16 channels are analysed one after another by means of an ADC giving channel advance instruction at the C_p input of IC-11.

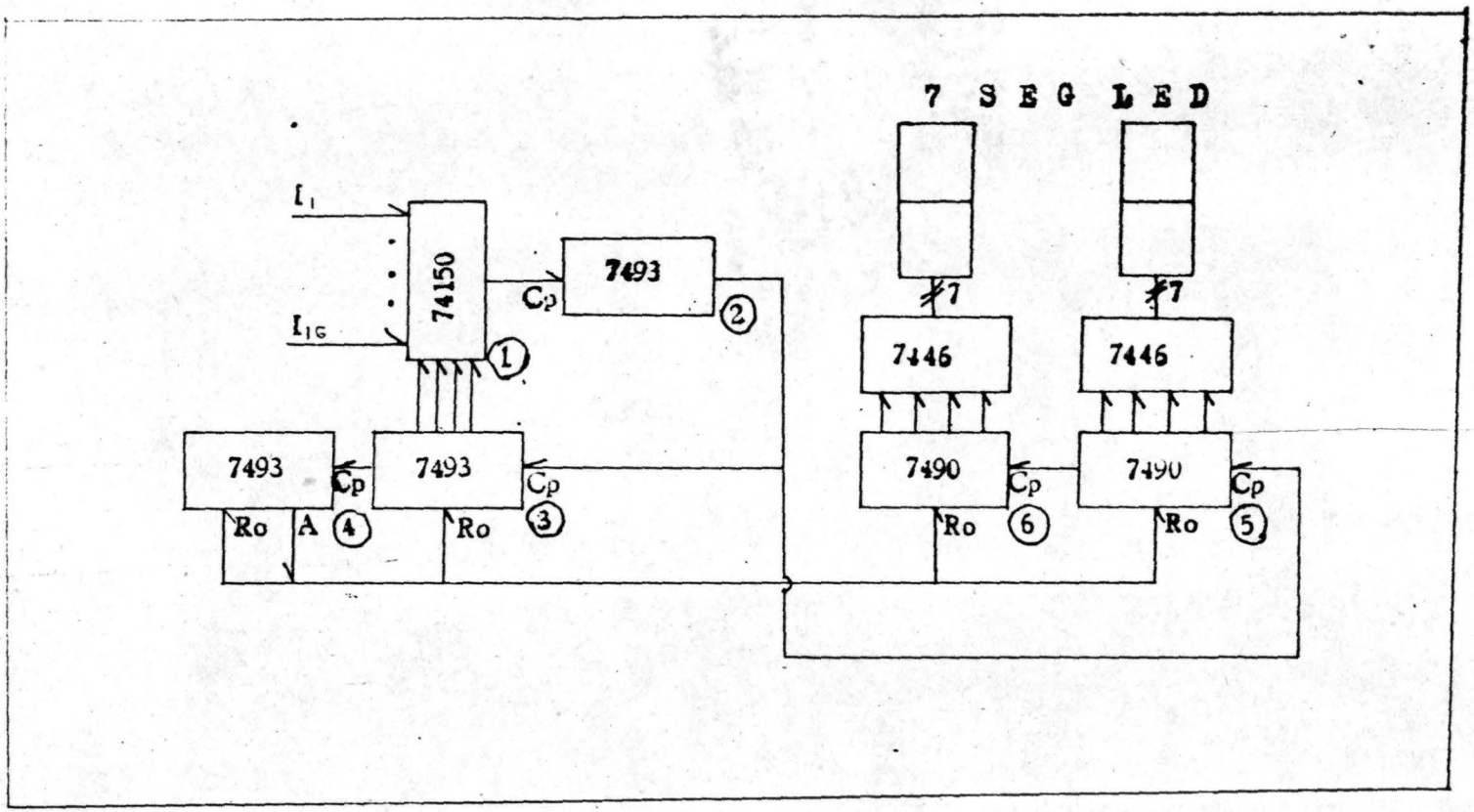

FIG-5.6 MONITOR UNIT

During the whole cycle of operation, the input line is closed and therefore IC-6 will not be triggered which in turns keeps 'B' input of IC-7 high. The input 'A' of IC-7 is permanently at low. Hence withdrawal of the hold 'command' makes a low to high transition of R_D of IC-7. This transition of R_D when 'B' input is high and 'A' input is low triggers IC-7 to discharge the capacitor C.

The storage capacitor C should be large to avoid error due to leakage when it is allowed to hold the voltage for a long time which an ADC takes to scan all the voltages standing at 16 channels or even more when multiplexed. Optimum value of capacitor is chosen at 0.02 μF to avoid 'over shoot'. During sampling the discharge of the capacitor C can be done by means of a silicon transistor by connecting its base directly to the Q output of IC-7 instead of using FET. But with silicon transistor the time of discharge of the condenser C is large compared to a FET as shown in fig. (5.7). The portion 'a' in fig. (5.7) gives the width of the sampling pulse in an arbitrary scale and the two curve 'b' and 'c' give the discharge through silicon transistor and FET respectively. At a particular time, indicated by dotted line AB, if there is a 'hold command', unit will hold the voltage present at that instant across the capacitor C by resetting IC-7. Thus by using silicon transistor the channel will give an information of voltage equal to the level A in absence of any pulse in that channel. Therefore in a fast detecting system FET is always preferable than a silicon transistor. High slew rate operation amplifier is used to multiplex the voltage to the

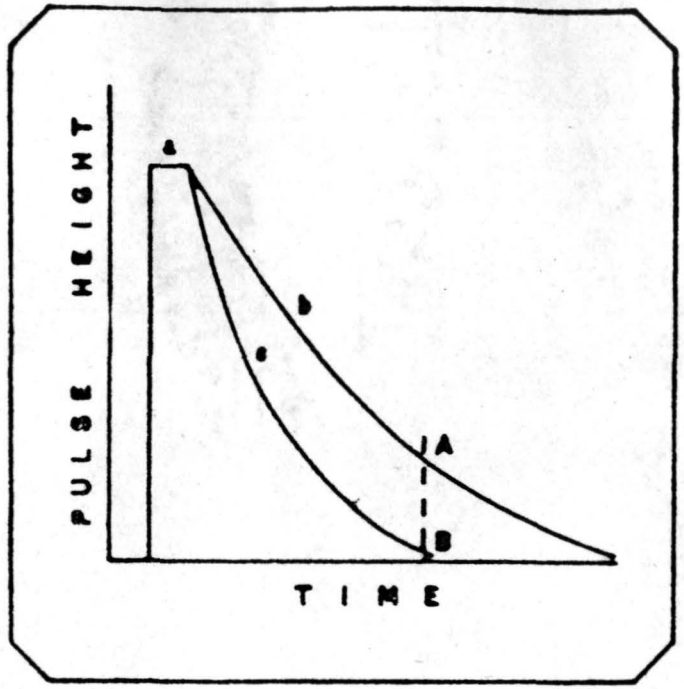

FIG. 5.7

CURVE SHOWING THE DISCHARGE OF THE STORAGE CAPACITOR BY A SILICON TRANSISTOR AND A FET. (a) WIDTH OF THE SAMPLING PULSE.
(b) DISCHARGE THROUGH THE SILICON TRANSISTOR.
(C) DISCHARGE THROUGH THE FET.

output for making the voltage setting time minimum. It is observed that the voltage setting time of the analogue multiplexer is less than 10 /us.

5.7 Monitor Unit

A continuous check of the amplifier output pulses coming from the density detectors for all the channels is made by monitor unit (fig. 5.6). The monitor is made by the pulses that are sampled at the 'Sample and Hold' unit. The triggering pulses of the 'Sample and Hold' unit during sampling to discharge the storage capacitor is multiplexed by IC-1 and connected to a 'divided by 16' counter IC-2. The output of IC-2 is connected to the C_p input of IC-3 acting as the address of IC-1 and decade counter (IC-5, IC-6). The QA output of IC-4 is used to reset the address register and the decade counters. The seven segment LED connected to the decade counter through decoders gives the digital display of the address of IC-1. When IC-1 is at a particular address it receives 16 pulses before it changes to its next address. Therefore the speed of change in address as is observed in 7 segment LED gives an idea of the rate of pulses coming from that channel. If the change in address approximates the single particles rate over the entire area of the detector calculated on the basis of cosmic ray flux then the channel may be taken as correct. If no pulse comes from a particular detector due to a fault in the circuit at any stage upto the amplifier, the address will not change and the monitor will stop at that particular address. Therefore the digital display indicates the faulty

channel number. Thus a continuous change in the digital display of the monitor with proper speed shows the correctness of all the channels.

5.8 Analogue to Digital Converter (ADC)

The digital encoding of pulse height in nuclear pulse height techniques with the method of Wilkinson[8] for digital measurements has succeeded over some other methods for digitisation of analogue pulses. Manfredy and Rimini[9], among others, have described a Wilkinson type analogue to digital converter (ADC) based upon the method of linearisation of the discharging process of a storage condenser. The method of Wilkinson has been used in the present work[10] to design a new analogue-to-digital converter based upon the technique of linearising the charging process of a condenser for use in cosmic ray air shower experiments.

5.8.1 Principle of operation

The operation of the converter starts with the charging of a condenser by means of a constant current source (linear ramp generator) to a voltage equal to the input pulse amplitude to be measured. The charging time of the condenser to a voltage equal to the input voltage is measured by means of 1 MHZ clock pulse. The operating principle is indicated in fig. (5.8). As the condenser voltage rises linearly to the input voltage, the number of clock pulses counted during the capacitor charging time is therefore proportional to the input voltage. The new design

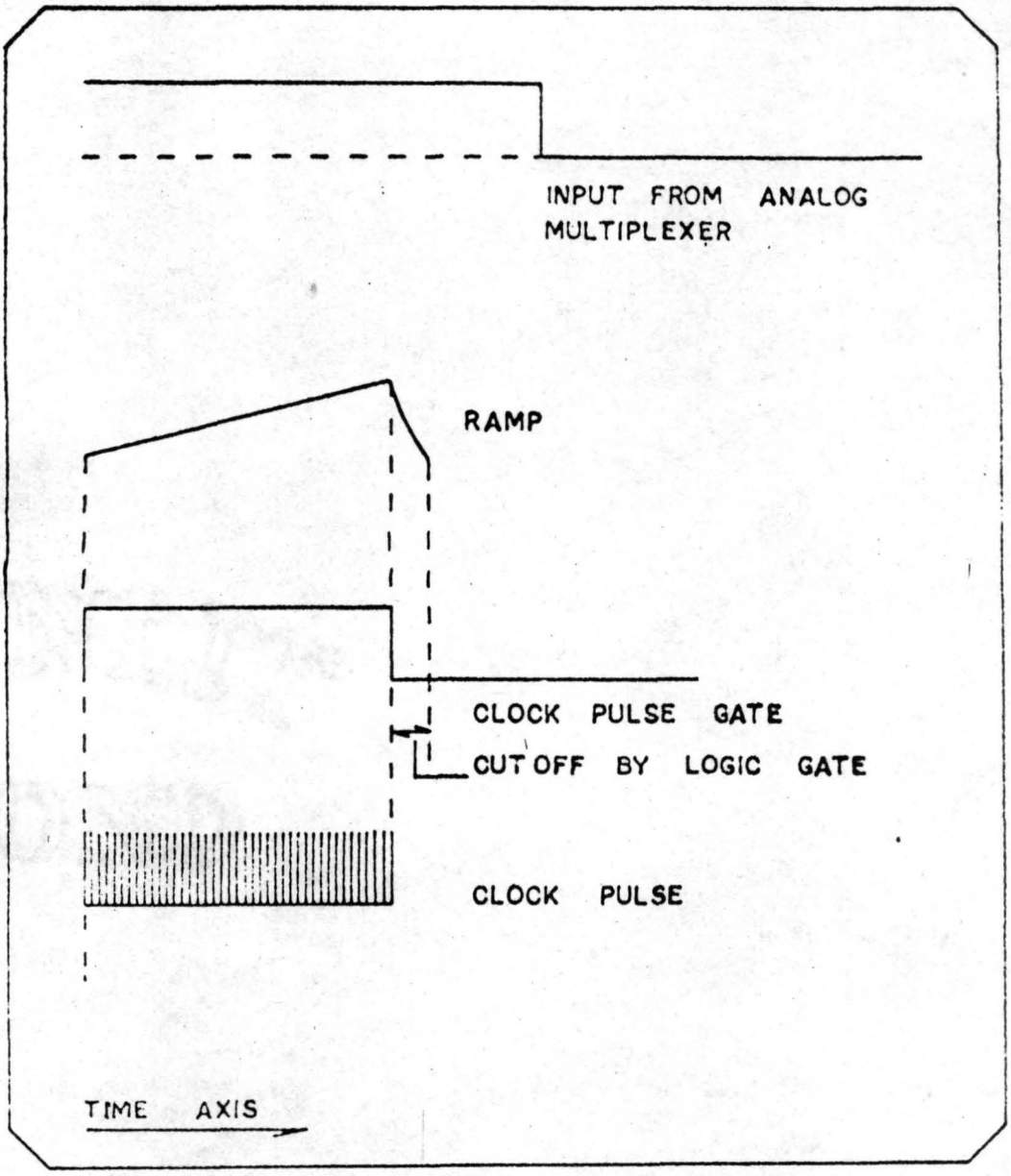

FIG. 5.8 PRINCIPLE OF THE ADC

for the realisation of the converter is described in the following section.

5.32 Description of the Converter circuit

This circuit diagram of the converter is shown in fig. (5.9). The whole circuit consists of two parts : (1) the ADC consisting of four operational amplifiers, two silicon transistors (T_1, T_2) and two TTL ICs(Ic-5, Ic-6), (2) a built-in-programmer consisting of logic gates and counters indicated in fig. (5.9).

In the ADC circuit the transistor T_1 acts as a constant current source to charge the capacitor C connected to the collector of T_1 and T_2. The voltage follower IC-1 connected to the capacitor C is meant to give information about the voltage across C to the comparator Ic-3. The transistor T_2 acts as an analogue switch across the capacitor C.

The analogue input pulse is fed to the comparator through a summing amplifier. The inverting input of the amplifier is connected to a preset for setting the output of the comparator at a zero logic level when the input voltage is at zero level. This occurs due to low voltage on the collector of T_2 in the conducting state. The output voltage of the comparator IC-3 is clipped a high logic level and connected to the input of an inverting logic gate G_1. The output of the invertor is connected to 'Reset to Zero' (R_0) input of a decade counter, IC-5. The output of G_1 is further inverted by G_2 and then applied to one of the inputs of the trigger controlling gate G_3. This input, directly related to the voltage setting time of the Analogue

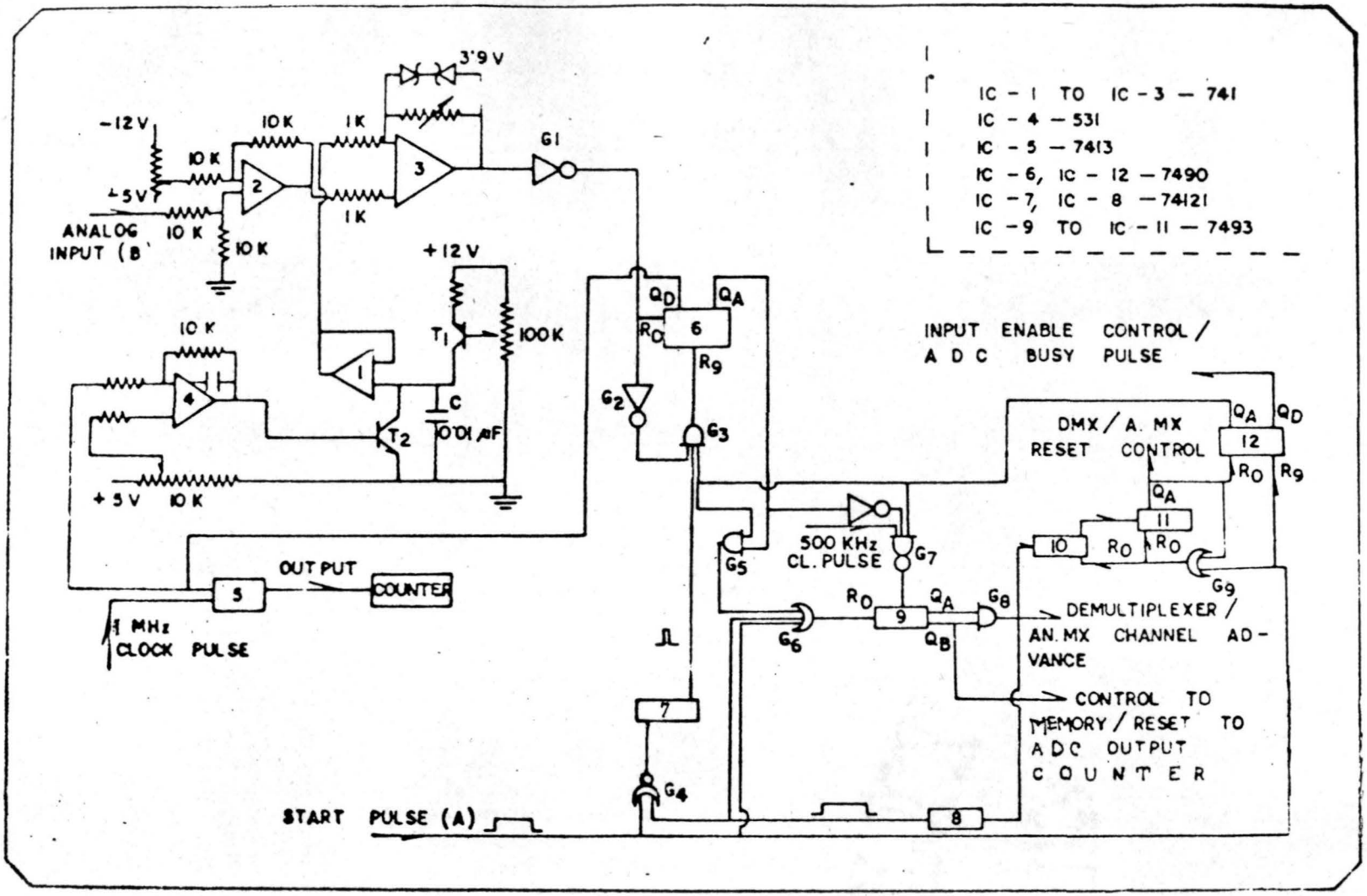

FIG. 5.9 CIRCUIT DIAGRAM OF THE ANALOG-TO-DIGITAL CONVERTER UNIT.

Multiplexer, will not allow any start pulse to the ADC until the voltage is set for scanning. The output of the gate G_3 is connected to the 'Reset to Nine' (R_9) input of the IC-6 whose output Q_A and Q_D are used to control the ramp generator as these two change their logic states with R_0 and R_9. Here decade counter (IC-6) is used for 'preset' and 'clear' purposes. Any flip-flop with 'preset' and 'clear' can be used instead of IC-6. But such a flip-flop should be properly gated so that when any one of 'preset' and 'clear' goes low the other should remain high. But in case of decade counter no such gate is necessary. The output Q_D of the IC-6 is connected to one of the inputs of the Schmitt trigger IC-5 containing a 1 MHz clock pulse and also the inverting input of the high speed operational amplifier IC-4 of unit gain. Instead of a Schmitt trigger (IC-5) a simple AND gate can be used provided the input 1 MHz clock pulse is a Schmitt triggered output to avoid errors that may occur in the counters which follow the ADC and which are very susceptible to noise. The output of IC-4 is connected to the base of T_2. The non-inverting input of IC-4 is connected to a 10K Ω resistor preset to apply a positive $\sim$ 1 volt so that when Q_D of IC-6 is high the base of T_2 goes negative, and when Q_D is low the base of T_2 goes positive just to make T_2 conducting. The output of IC-5 gives the serial data output which can be connected to counter for parallel data output.

The built-in-programme is an assembly of different logic gates (G_3 - G_9), counters (IC-9 to IC-12) and monostable multivibrators (IC-7, IC-8). The monostable multivibrator IC-7 triggers the ADC and IC-8 allows the voltage setting time of

analogue multiplexer. For analysis with 16 channels, the output Q_A of IC-11 is used to reset the analogue-multiplexer, demultiplexer, address register, the preset counters (IC-10, IC-11) and programme controller IC-12.

5.8.3 Operation of the circuit

The unit IC-12 which controls the whole programme is normally reset to zero and the ADC will not scan any input voltage applied at the analogue input terminal B. Whenever there is an input voltage to be measured, a positive start pulse derived from the control unit is applied to the 'start pulse' input terminal A. The width of the start pulse is slightly greater than the voltage setting time of the analogue-multiplexer with its output point connected to the analogue input terminal B. The positive edge of the start pulse resets the IC-12 to nine (R_9) and IC-9, IC-10 and IC-11 to zero (R_0) through gates G_6 and G_9. The output Q_D of IC-12 after being inverted connects the analogue multiplexer and demultiplexer [fig. (5.10)] to the ADC through 'input enable control' and the output Q_A of IC-12 sets one of the inputs of gates G_3 and G_7 high. The input voltage makes comparator IC-3 output high making R_0 of IC-6 low. The IC-7 is triggered at the end of start pulse to reset IC-6 to nine (R_9) so that Q_A and Q_D of IC-6 are high. The width of the triggering pulse must be less than 1 /us for 1 MHz clock pulse. The output Q_D makes the base of T_2 negative and opens the 1 MHz clock pulse to the ADC counters and the storage capacitor starts charging at a constant current via T_1 until the output of comparator IC-3 goes to zero logic level making R_0 of IC-6 high. As R_0 of IC-6 goes high, the output Q_D.

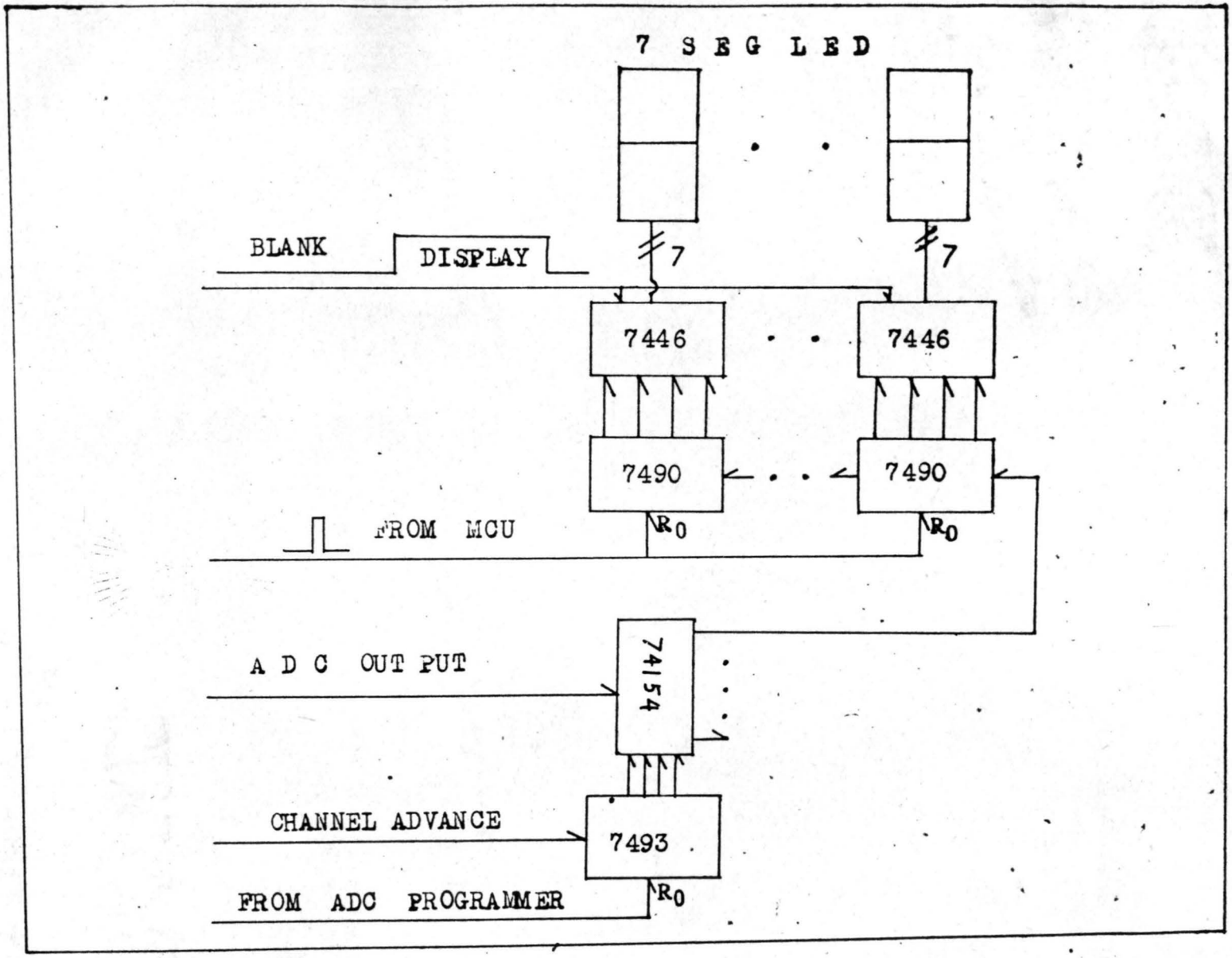

FIG-5.10 DEMULTIPLEXER AND DISPLAY UNIT

of IC-6 becomes low stopping 1 MHz clock pulse to the counters and making the base of T_2 positive to enable the capacitor C to discharge. Here the transistor T_2 is switched on and off by an operational amplifier (IC-4) but not by conventional TTL levels. This is done for the reason that logic low level sometimes give $\sim$ 0.1 volt or even $\sim$ 0.2 volt. It is observed that there is low conduction current through the transistor T_2 which affects the linearity between the digital output and the analog input. Replacing T_2 by a field effect transistor (FET) BFW-11 gives better result. With BFW-11 the gain of IC-4 is made about 3 so that when Q_D of IC-6 is low the gate of BFW-11 goes to about 1 volt and when Q_D is high the gate goes to less than - 4 volts which is equal to the drain current cut off voltage for BFW-11. At the end of the conversion, the discharge of the capacitor C takes place through the FET. The FET being a better electronic switch than a silicon transistor, the discharge of the capacitor C is very fast to make the ADC ready for the next scan. The output Q_A of IC-6 being low, the output of G_5 is low. As there is no start pulse either at the input A or from IC-3, the output of G_6 is also low, making R_0 of IC-9 low. The 500 KHz clock pulse now enters the counter IC-9. The output Q_A and Q_B of IC-9 through G_3 increases the preset counter reading and the analogue multiplexer and demultiplexer channel address by unit and produce another start pulse at the monostable multivibrator IC-3. As soon as the start pulse is generated, R_0 of IC-9 goes high through G_5 and the 500 KHz clock pulse entry to IC-9 is cut off starting a new cycle of operation. At the end of the sixteenth cycle, the output Q_A of

IC-11 goes high, thus resetting the preset counter and the programme controlling IC-12 to zero, making the whole system ready for a new cycle of operation.

The circuit described above is standarised and is operated in the air shower experiments. The voltage ramp has a fairly constant slope and good linearity up to 10 V. For a charging current corresponding to 10 mV/μs, the differential non linearity is $< \pm 1\%$ for an input voltage higher than 50 mV but less than 10 volts. Linearity above 10 volts can be achieved by operating the transister T_1 with a higher voltage (15 volts).

A 1 MHz quartz oscillator is used in the test circuit. The clock oscillator and the ramp generator are controlled by logic gates and hence all possible errors at small input voltage are expected to be negligible. Since R_9 overrides R_0, there may be an inaccuracy at zero input voltage of one channel width if the start pulse to IC-6 synchronises with the high logic level of the clock pulse. This can be avoided by interchanging 'reset to nine' (R_9) with 'reset to zero' (R_0) and by inverting outputs Q_A and Q_D of IC-6.

Fig.(5.11) shows the relation between the digital output and the analogue input. The digital output of the ADC for a particular height of an analogue pulse is not constant but can be adjusted. To fix the digital output at a particular value the bias of the transistor T_1 is adjusted which controls the charging rate of the capacitor C. For a digital output 100 per volt with 1 MHz clock pulse the conversion time is 100 μs/V. But using a 10 MHz clock and adjusting the digital output 100 per volt the

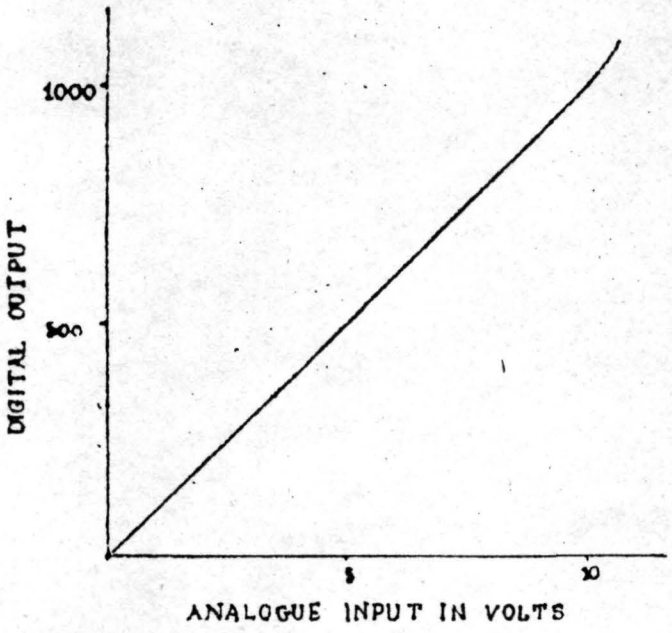

FIG. 5.11 RELATION BETWEEN THE DIGITAL OUTPUT AND THE ANALOGUE INPUT.

conversion time becomes 10 /us/V. In both cases the resolution is 10 mV. This resolution can be made 1 mV by making the digital output 1000 per volt by adjusting the charging rate of the capacitor C through transistor T_1. In this case the conversion time becomes 100 /us/V using a 10 MHz clock pulse. It may be mentioned that all operational amplifiers 741 should be replaced by 715. This is the main advantage of the ADC where we can adjust the conversion time and resolution according to need.

5.9 Random access memory with programmer for data acquisition and printing in a multidetector system

Random Access Memory (RAM) is extensively used in storing the programming information in a computer and micro system and data storing in multichannel and multi scaler analyser. In the present form of the circuit are used to first store the digital information of scintillator pulse height and then printed by means of a line printer on a paper tape.

5.91 Description of the circuit

The fig. (5.12) representing the circuit diagram of whole system. The four IC (IC-1 to IC-4) are 1K (4 x 256) random access memory (MOS). IC-5 to IC-8 are the decade counters to accept the serial data output from ADC with a programmer. IC-9 and IC-10 are to address the memory channel. The output from the memory are not directly connected to the printer but through NAND gates serving the purpose of multiplexer to accommodate data from other source (i.e., magnetic spectrograph unit). Insted of NAND gates two line to one line multiplexer can also be used. IC-11

to IC-23 together with set reset latches and number of gates constitute the programmer which controls the writing of the whole information in the memory and then gives the print command to the line printer to print all the information in the memory. The programmer also makes the provision to connect the magnetic spectrograph memory unit to the line printer to print the digitised neon tube glow information. IC-11 is used to reset the ADC output counters and to advance the memory channel by unity delayed by IC-12 when the write-command for each channel is withdrawn. IC-13, 14, 18, 19 acts as preset counters to control the number of data to be printed from magnetic spectrograph unit and from memory unit. IC-15, 16, 20, 21 are retriggerable monostable multivibrators whose triggering is controlled by set-rest latches R/S-1 and R/S-2 and give the 'print in red' and 'print in black' command when the writing in the memory is over and IC-17 initiates the 'print in red' command when the 'print in black' is over. All the inputs to the memory and the programmer are outputs from the ADC with the programmer (fig. 5.9).

5.92 Operation of the circuit

Whenever there is an event to record, the operation of the circuit is initiated by means of a 'start pulse' from the master control unit (MCU) applied at the inputs of the gates G_1 and G_2. This start pulse first reset all the counters IC-5 to IC-8 to zero through G_9 and makes R_D of IC-20, 21 low through R/S-1 to make it nontriggerable. The output of all memory ICs are gated off by R/S-1 through G_3. The 'enable control' is held high from ADC programmer. As the "enable control" is high, the output of G_8

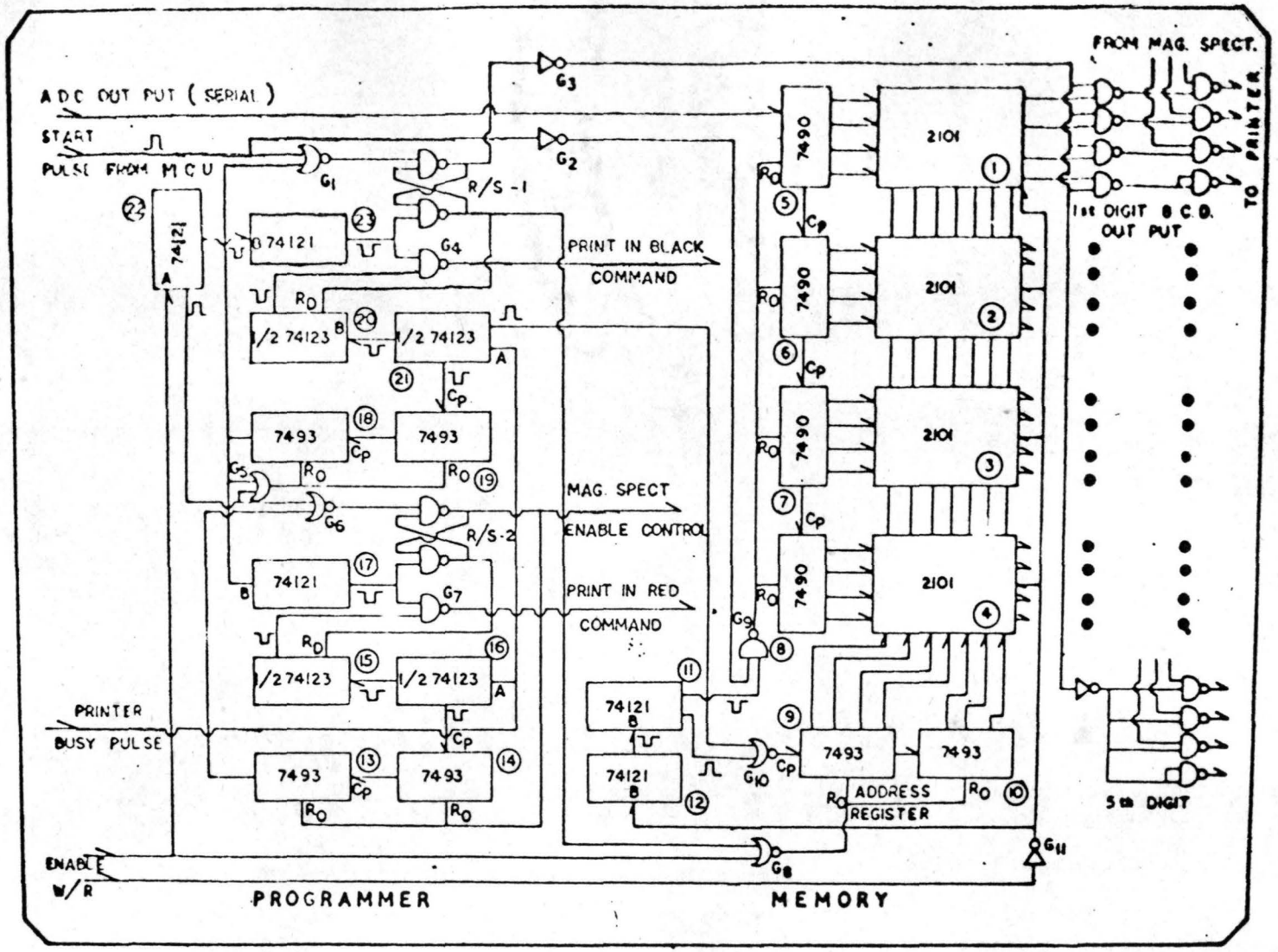

FIG. 5.12 RANDOM ACCESS MEMORY WITH PROGRAMMER.

which controls the R_0 of memory address register is low for addressing the memory. At the end of start pulse ADC scan is started and the serial data output from the ADC enters the decade counters (IC-5 to IC-8). When the ADC scan for the 1st channel is over the ADC programmer gives a write-pulse to the memory. This write pulse is greater than 1 /us which is equal to the minimum writeaccess time of a MOS memory. When the write pulse is withdrawn it triggers IC-12 which in turn again triggers IC-11 to reset the decade counters and to increase the address of the memory by unity. As the MOS memory does not operate with TTL speed so far as the read and write mode is concerned the resetting of the decade counters and the advancing of the address are delayed by some fraction of micro second. This delay in the measurement of digital information of the pulse height will not affect the speed of operation since the analogue multiplexer (fig. 5.5) which connects the ADC to the second detector output pulse always takes some time termed as 'voltage setting time'. The ADC scan for second channel is now started and is stored in the corresponding address of the memory as was done in the first channel. When the ADC scan for all the channels are over the enable-control goes low which sets the memory at zero address through G_3 and triggers IC-22. The width of the pulse from IC-22 should be greater than 1 /us which is equal to the read-access time of the memory and also determines the time after which the printing will start. The output from IC-22 resets the preset counters (IC-18 and IC-19) through G_5 and operates R/S-2 to make R_0 of preset counters (IC-13 and IC-14) high and R_0 of IC-15 and IC-16 low. IC-23 is

triggered by IC-22 to give a 'print in black' command to the printer and to operate R/S-1 to connect the memory output to the printer through multiplexer and to make R_D of IC-20 and IC-21 high. As soon as the printer gets the print command 'printer busy pulse' goes high and at the end of print 'printer busy pulse' goes low and it triggers IC-21 which advances the memory-address and preset counter by unity and triggers IC-20 to give an another 'print in black' command. At the end of the required number of printing the preset counter operates R/S-1 to stop the triggering of IC-20 and IC-21 by making R_D low and to switch off the memory output and to connect the magnetic spectrograph memory unit (fig. 5.14) to the printer. The preset counter also triggers IC-17 that gives a 'print in red' command to the printer through G_7 and operates R/S-2 to makes R_D of IC-15 and IC-16 high. It also makes R_D of IC-13 and IC-14 and the enable control of magnetic spectrograph unit low. As in the case of 'print in black' command 'print in red' command is generated by IC-15 and IC-16 controlled by the preset counters (IC-13 and IC-14). After the end of print of the whole information preset counters (IC-13 and IC-14) operating R/S-2 stops further printing by making R_D of IC-15 and IC-16 low. The preset counter is also resetted to zero and the whole system is ready for next event.

The important feature of the circuit is that one should be careful about the speed of operation of the MOS memory when it is operated by TTL ICs. Generally the read and the write access time of a MOS memory is greater than 1 μs. Therefore a

print command to a printer whose interface operates with TTL ICs to print the information from the memory should be delayed by a minimum time of 1 /us after the change of address so that the printer interface gets the information of valid data output from the memory. For this reason the pulse width from IC-21 and IC-16 must be greater than 1 /us. In storing the data in the memory 'write-pulse-width' should also be greater than 1 /us. The resetting of the counters at the data input points and the change of address register of the memory should not be made simultaneously with the withdrawl of the write pulse but after a definite interval of time depending upon the memory characteristics. For this reason triggering of IC-11 is delayed by IC-12 after the withdrawal of the write pulse and this delay time may be some fraction of micro second.

5.10 Memory Unit of magnetic spectrograph

To avoid the tedious method of recording and scanning by photographic method Ayre and Thompson[11] (1969) had developed an electronic method of recording tube flash. The simple method is shown in fig. (5.13). A brass screw acting as a probe was placed close to the window of each flash tube and pulse with several-hundred volts with polarity as that of the EHT pulse was obtained accross the register R when the tube flashes. It was shown by Ayre and Thompson[11] (1969) that output pulse mainly depends on the register R. By tapping off a suitable portion of R the tube glow can be recorded in a solid state device. This method was successfully used by Durhum University in their MARS spectrograph. The preliminary investigation shows that an effective

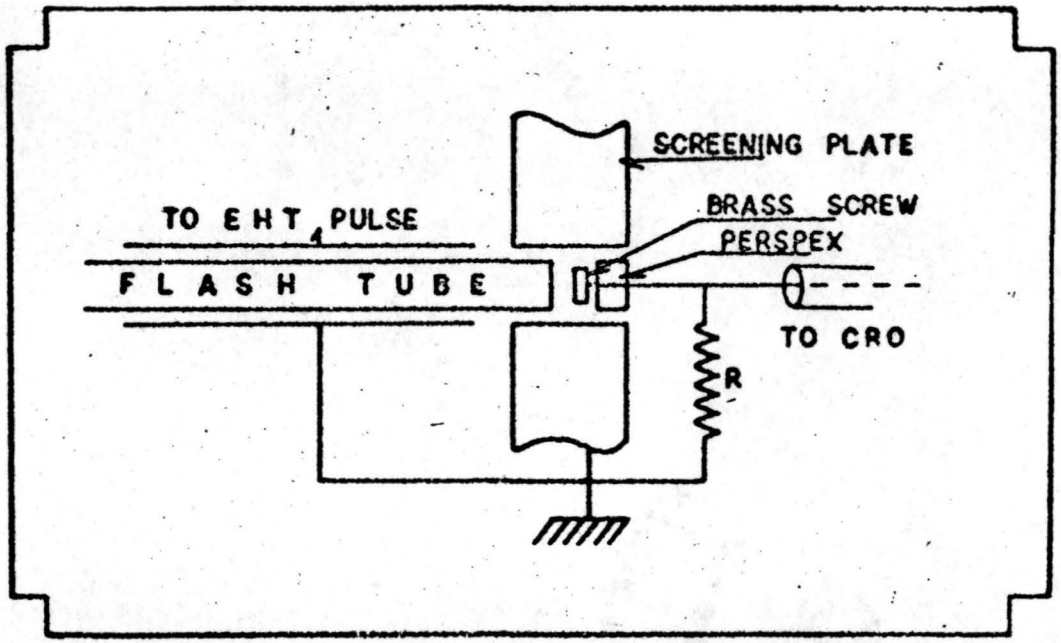

FIG. 5·13 ELECTRONIC METHOD OF RECORDING TUBE FLASH.

probe pulse is obtained by proper shielding of the flash tube trays of the magnetic spectrograph.

The recording of the neon tube probe pulse by the method of Ayre and Thompson (1969) is shown in fig. (5.14). The probe pulse from all the tubes are first stored by means of 'Set-Reset' (R/S) data latch the number of which is equal to the number of neon tubes. The output of R/S is fed to shift register (Parallel load serial shift) acting as memory. The tube information of all the layers are fed to shift register in such a fashion that a particular tube number, say the first tube, of each layer is made serial to give the corresponding binary bit to the printer. Since the total number of tubes in each layer is 15 all the tubes are made serial in 15 rows to record all the tube information. These 15 outputs are connected to the printer in Octal system. Each flash tube tray in magnetic spectrograph consists of eight layers, each layer contains fifteen tubes. These fifteen tubes are divided into five groups, each group containing three tubes. Each group as three-tube information is fed to the line printer as binary information A, B, C for digital print. The D input is kept low. Hence if the glow is recorded with logic high, the five digits corresponding to fifteen tubes printed by the line printer will give the tube glow information as illustrated in the table 1.

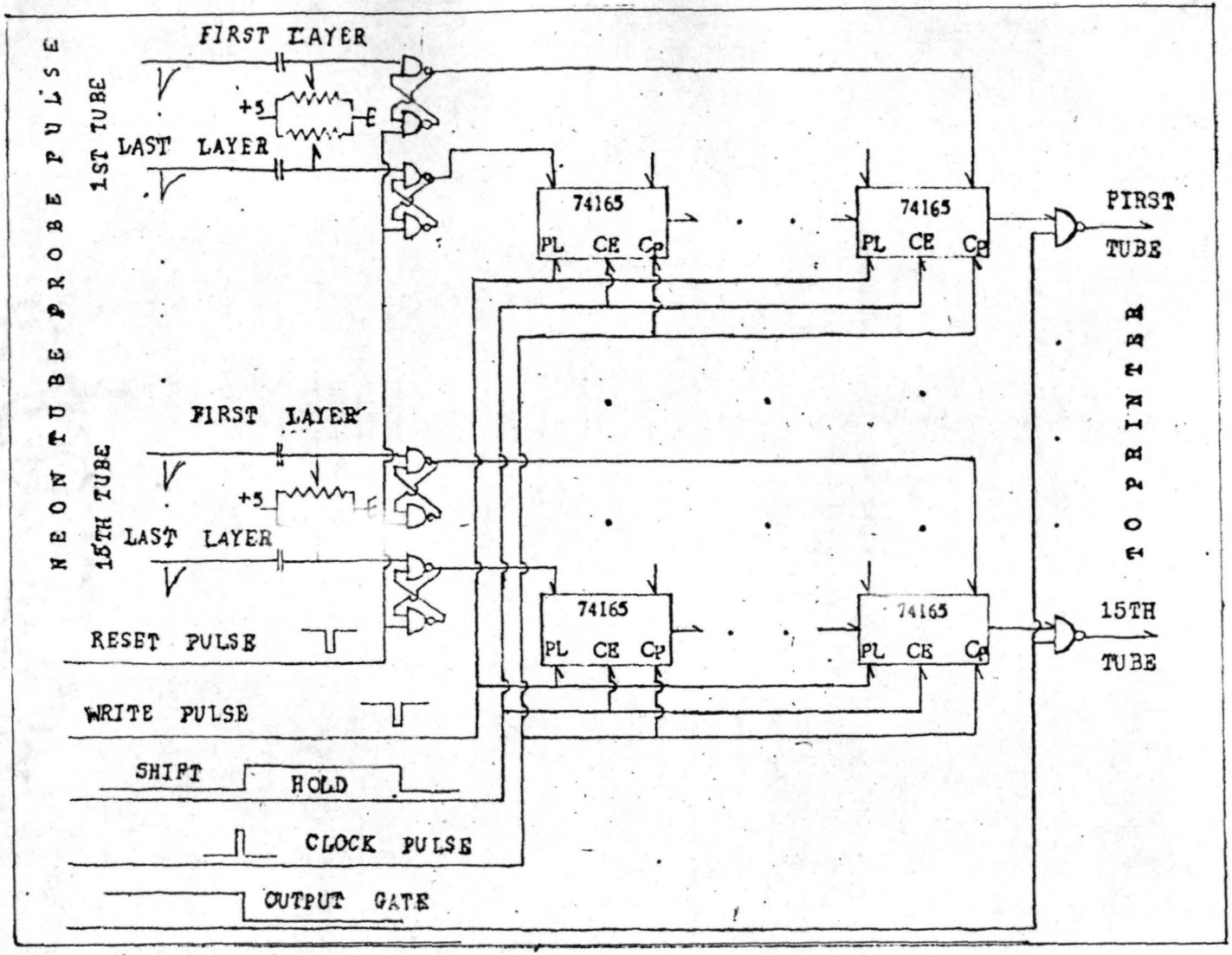

FIG- 5.14 CIRCUIT DIAGRAM OF THE MEMORY UNIT OF THE MAGNETIC SPECTROGRAPH.

Table 1

Tube Glow	Information at the input of the line printer					Digital output
3rd	001	000	000	000	000	10000
2nd and 3rd	011	000	000	000	000	30000
3rd and 6th	001	001	000	000	000	11000
3rd and 4th	001	100	000	000	000	14000
2nd, 3rd, 4th and 5th	011	110	000	000	000	36000

The probe pulse input point of all the R/S latches is gated to high logic state. To start with all the outputs of the R/S latches are resetted to zero by making reset input low. In case of an event to record whenever there is a tube glow information for a number of tubes giving a negative pulse at the probe, the output of R/S latches corresponding to those tubes goes high. A write pulse from master control unit gives a parallel load to the shift register. At the end of write pulse all the output of the R/S latches are again resetted to zero. The start pulse from the master control unit gives a hold command to the shift register through memory programmer. At the end of the pulse height analysis by the ADC the printer starts printing of the digital pulse heights by making the output gate low. At the end of the pulse height print 'hold command' is withdrawn and the output gate is made high by the memory programmer and the printer starts printing of the digitised neon tube glow information by giving clock pulse to the shift register by the memory programmer. The clock pulse gives a

serial shift to the shift register. First print gives the first tube layer information for 15 tubes. After the first print the clock pulse transfers the second tube layer information to the printer. Thus each layer information corresponds to each line of printing. After the end of the printing of all the tube layer information the whole system is ready for the next event.

5.11 Measurement of single particle pulse height and the efficiency of the plastic scintillators.

The plastic scintillation counters in the air shower array gives the information of particle density. The pulse height of the detector is proportional to the number of particles incident on the counter. The single particle pulse height over the entire area of the detector may or may not be the same which depends on the size of the scintillator. Therefore the measurement of single particle pulse height and efficiency of the detectors are necessary for the measurement of particle density.

To measure the single particle pulse height, each scintillation counter is placed along a line of alignment of G.M.counter telescope as shown in fig. (5.15). Out of three G.M. counter one is crossed and the scintillation counter is placed in such a way that if a charged particle passes through the four counter it produces four negative pulse at the output of four counters. The three G.M.pulses are used for the coincidence. For the measurement of pulse height the coincidence pulse from the three G.M.counter is used to trigger the master control unit and the output from the plastic scintillator is connected to the

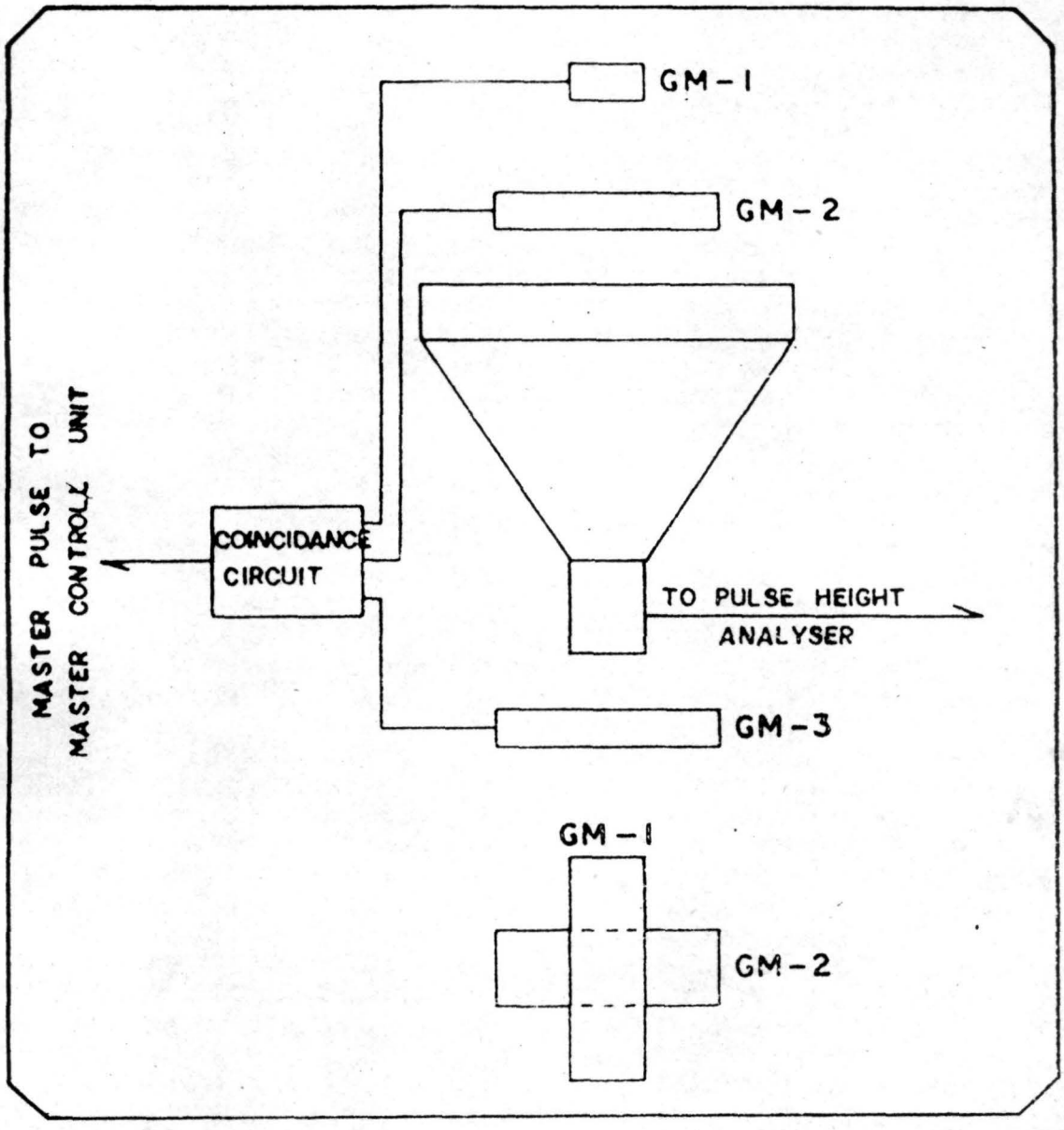

FIG-5.15 ARRANGEMET FOR MEASURING SINGLE PARTICLE PULSE HEIGHT

first channel of the pulse height measuring circuit. By this arrangement the experiment was conducted for a long time. The digitised output represents the scintillation counter pulse height. Fig. (5.16) shows the histogram of the single particle pulse height when the particle passes through the central region of the scintillation counter. The experiment is repeated for all the detectors and the digital output for single particle pulse height is made the same for all the detectors by adjusting the high voltage of the photomultiplier tube.

The digital output for single particle pulse height is 45 as is seen from fig. (5.16). Since the ADC is calibrated a digital output 100 per volt, the single particle pulse height at output of the last stage amplifier is 450 mV. The output pulse of P.M.tube is amplified 300 times before it reach the ADC for scan. So the mean single particle pulse height at the output of P.M.tube is 1.5 mV. The preamplifier gain is 30 and linear upto 10V and hence the dynamic range is equal to the maximum number of particles measurable without any loss of linearity is about 220 particles per detector.

To measure the efficiency of the detectors the plastic scintillators are shifted in such a way that a charged particle producing coincidence pulse in passing through the G.M. telescope passes through near the edge of the detectors. The experiment is repeated for different position of the scintillators. It is observed that the efficiency at center and at edge of the detectors is 100% and 92% respectively. The variation of efficiency fig. (5.17) is small (8%) due to small size

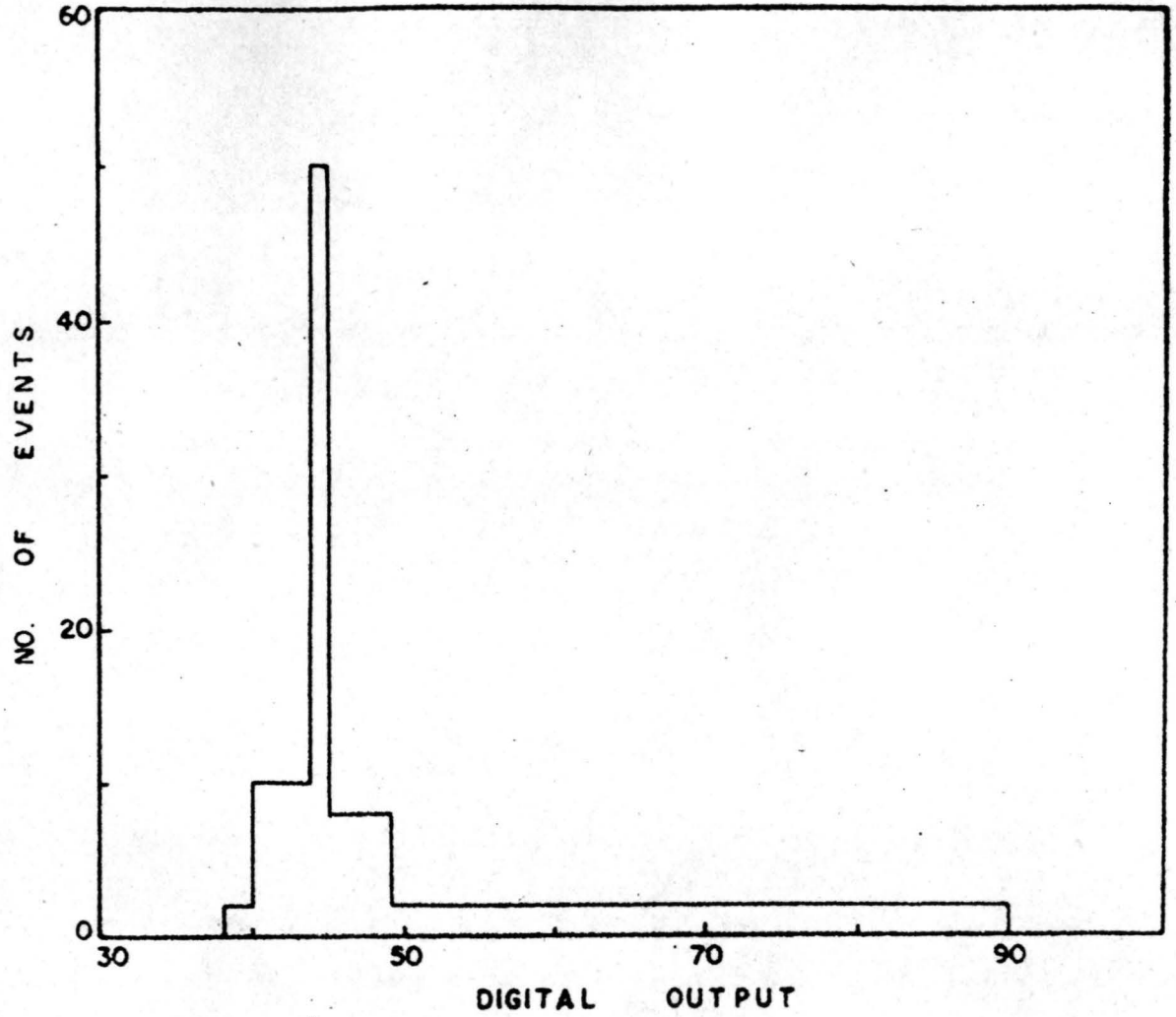

FIG. 5·16 HISTOGRAM OF THE SINGLE PARTICLE PULSE HEIGHT

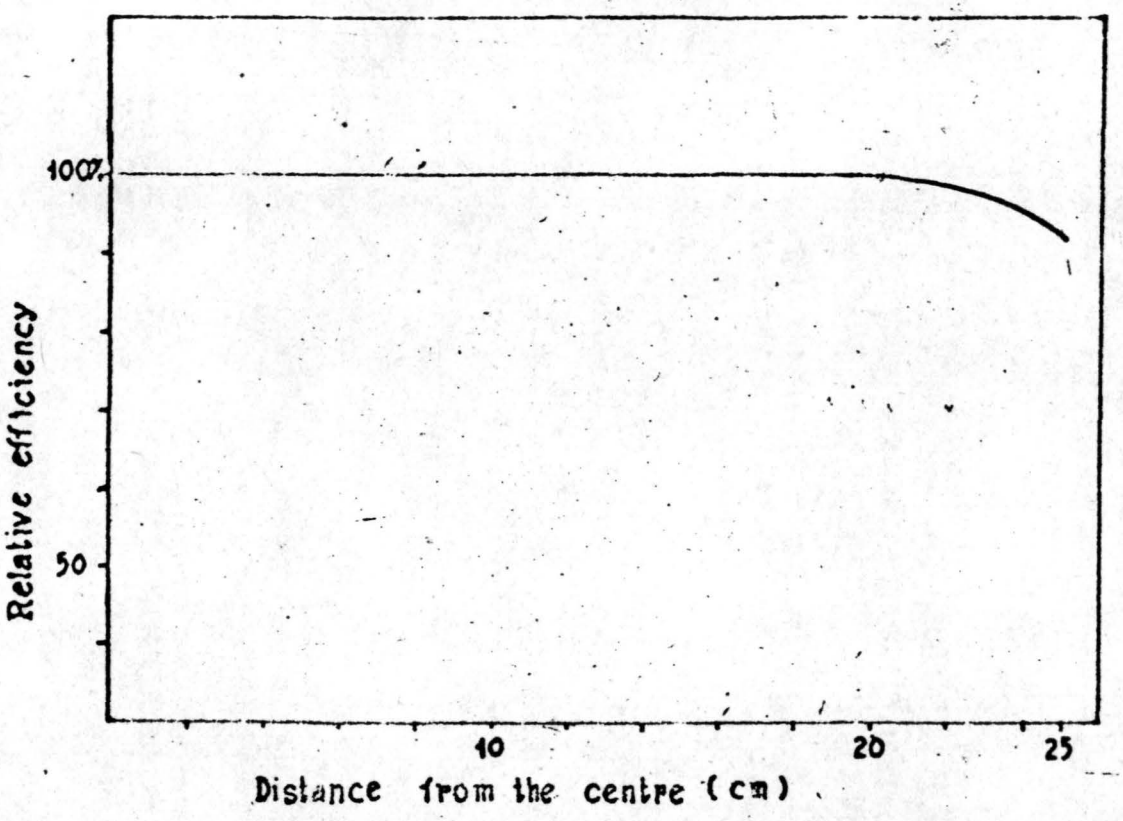

Fig. 5.17 VARIATION OF EFFICIENCY FROM THE CENTRE TO THE EDGE OF THE PLASTIC SCINTILLATOR

($\frac{1}{4}m^2$, $\frac{1}{8}m^2$) of the detectors.

5.12 Cross calibration of the channel

The amplifier used in the circuit are all operational amplifier. The gain of all the amplifier is 10. The ADC measures the output voltage of amplifier through sample-hold and analogue multiplexer, so it is necessary to check the digital output of all the channels with respect to the first channel for the correct operation of the circuit. For this a pulser unit is connected to the first channel and first channel is shorted with other channels one after another. The circuit is triggered by the pulse coming from the first channel (single fold triggering). The digital outputs for all the channels are compared. Fig.(5.18) shows the cross calibration curve.

5.13 Response of the Flash-tube chamber

To test the response of the flash-tube chamber three G.M.counter trays are used. One tray is placed at the bottom other at the top and the third one within the chamber in between the flash tube trays. The G.M. trays are placed vertically one after another. The coincidence pulse of the three G.M.trays are used to trigger the flash tube control unit to photograph the muon track. The experiment is repeated over the entire area of chamber. Photograph of the muon track through the chamber is shown in fig. 4.9 (Chapter IV).

5.14 Day to day maintenance of the circuit

The maintenance of the circuit is one of the major

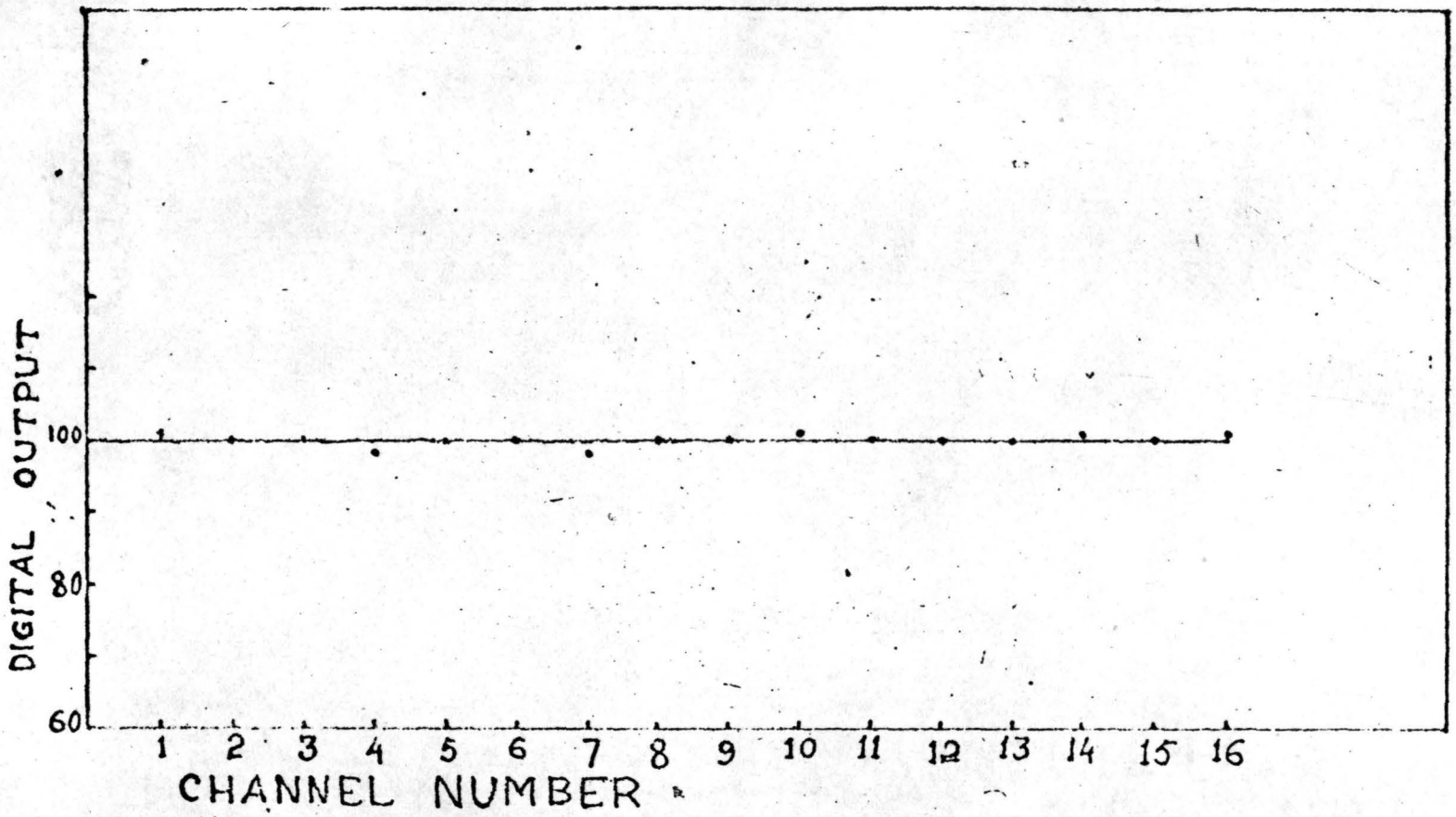

Fig. 5.18 CROSS CALIBRATION OF THE CHANNELS

task of the air shower experiment. The performance of the linear amplifier are frequently checked for drift in gain and linearity, so that correction are made when deviation occur, to maintain uniformity of response. The pulse shape, width etc. of all the channels are regularly checked by an oscilloscope in addition to the constant checking by the monitor unit. The sample-hold unit holds the peak of the analogue pulse for a few micro second by storage capacitors and any leakage in the storage capacitor is visually checked while regular runs are in progress. The function of the whole circuit are checked once a week by feeding known pulse height at the input and the digital output are taken from the printer on a paper tape. If there is any inconsistency arises between the input pulse height and the digitised output then we immediately check the gain of the amplifier, sample-hold unit and at last the ADC circuit. All the density detectors are checked once a month for the verification of single particle pulse height. For this, we use a vertical G.M.telescope for the determination of single particle pulse height which is described in section (5.11). If there is any shift of the single particle pulse height that can be observed from the histogram. This shift is mainly due to the change of preamplifier gain or due to the change of high voltage supply to the P.M.tubes. The original single particle pulse height is obtained by adjusting the preamplifier gain and the high voltage supply to their original value.

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