Chapter 6

BORDER COLLISION BIFURCATIONS IN ONE DIMENSIONAL DISCONTINUOUS MAPS OF PRACTICAL BOOST CONVERTER

6.1 Introduction

It has been found that most feedback controlled switching circuits exhibit nonlinear phenomena and chaos over significant parts of the parameter space. It has also been revealed that in addition to saddle-node bifurcation and period-doubling cascade, the feedback controlled switching circuits exhibit many atypical bifurcation phenomena. Generally the nonlinear dynamics of physical systems are analyzed by obtaining discrete models popularly known as maps. Due to the existence of periodic clock pulses in the control logic, the Power electronic circuits like boost converters are suitable for such discrete domain modeling. We can observe the states in synchronism with the clock pulses and develop a function that maps the states from one clock instant to the next. A map is said to be smooth if it has a continuous derivative and monotonic if there is no change in the sign of the derivative. It has been found that the discrete domain modeling of most switching circuits i.e., maps are piecewise smooth and piecewise monotonic [1]. In the paper[2], [14],[113],[114] the authors explored the dynamics of general piecewise smooth piecewise monotonic one dimensional (1-D) maps and apply the results in explaining the nonlinear phenomena in the boost converter without parasitic effect. In the paper [124] the authors explored the dynamics of general piecewise smooth piecewise monotonic one dimensional (1-D) discontinuous maps and apply the results in explaining the nonlinear phenomena in the boost converter without parasitic effect. Here we explore the dynamics of piecewise smooth piecewise monotonic one dimensional (1-D) discontinuous maps of Pure DC fed boost converter with parasitic effect and Rectified DC fed boost converter with parasitic effect.

The theory of border-collision bifurcations is developed for piecewise smooth maps in recent years by di Bernardo [2], Soumitra Banerjee [76] and others . They developed the form of the one dimensional maps is given below

$$f(x,y,\rho) = f_1(x,y\rho) \quad \text{for} \quad (x,y) \in R_1$$

$$f(x,y,\rho) = f_2(x,y\rho) \quad \text{for} \quad (x,y) \in R_2$$

$$f(x,y,\rho) = \text{----------} \qquad \text{----------(6.1)}$$

$$f(x,y,\rho) = \text{----------}$$

$$f(x,y,\rho) = f_n(x,y\rho) \quad \text{for} \quad (x,y) \in R_n$$

where R_1, R_2 are regions of the phase space with dividing borderlines and ρ is a parameter. It is assumed that the map is continuous but with a discontinuity across the borderlines. Investigation in this regard are reported in[3],[15],[46],[47],[72]-[75], [77]-[80]. A large class of practical systems in electrical engineering are modeled as piecewise smooth maps and border-collision bifurcations are common in them. A line of development shows that there are important classes of switching systems like thyristor circuits which yields discontinuous maps under discrete time modeling and nonstandard bifurcation phenomena can be there in such systems. The theory for understanding such bifurcation phenomena is developed by Parag Jain And Soumitra Banerjee [76]. In that paper they classified the border collision bifurcations that occur in one dimensional maps with discontinuity at the border. They also illustrated the application of the theory in practical example of a power electronic switching circuit with a delay in feedback loop(without parasitic effect).

6.2 The One-Dimensional Discontinuous Map

An 1-D map $f(x;\mu)$ that maps the real line R^1 to itself and depends on the parameter μ [122] . A point $x = x_b(\mu)$ divides on the real line it into two regions (fig. 6.1) R_A and R_B . The map $f(x;\mu)$ is piecewise continuous in the sense that it is continuous in (x ; μ) both the regions R_A and R_B , but is discontinuous at x_b . The one-sided limits of the partial derivatives of $f(x;\mu)$ exist at the border x_b. With all generality maps are considered whose partial

derivatives and the length of the discontinuity at the border are independent of the parameter μ. As we are concerned in the bifurcations that occur when a fixed point crosses the point of discontinuity x_b, we study these through the piecewise linear approximation in the neighborhood of the border:

$$x_{n+1} = ax_n + \mu \quad \text{for } x_n \langle 0$$

$$x_{n+1} = bx_n + \mu + l \quad \text{for } x_n \rangle 0 \quad \ldots\ldots \quad (6.2)$$

and the state space is divided into two halves L (left) and R (right) and l is the length of the discontinuity. A movement of the break-point is introduced towards the origin by transformation of coordinates. The fixed point in L is located at $x_L^* = \frac{\mu}{1-a}$ and that in R is located at $x_R^* = \frac{\mu + l}{1-b}$. The map intersects the 45^0 line for $\mu < 0$ and $\mu > -l$. It indicates that the fixed points collides with the border at $\mu = 0$ and $\mu = -l$. So two border collision events are expected as the parameter μ is varied.

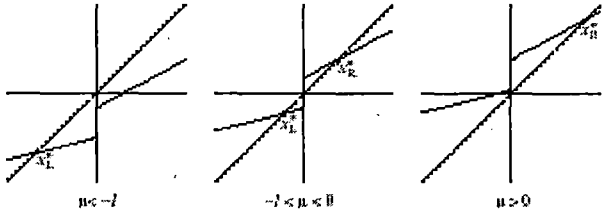

Fig. 6.1 Graphs of the map for $0\langle a\langle 1$, $0\langle b\langle 1$ and $l\rangle 0$

Different classification are made on the basis of different ranges of a and b.

Case 1: $0\langle a\langle 1$ and $0\langle b\langle 1$

Case 2: $0\langle a\langle 1$ and $b\rangle 1$

Case 3: $0\langle a\langle 1$ and $-1\langle b\langle 0$

Case 4: $0\langle a\langle 1$ and $b\langle -1$

Case 5: $a\rangle 1$ and $b\rangle 1$

Case 6: $a\rangle 1$ and $-1\langle b\langle 0$

Case 7: $a\rangle 1$ and $b\langle -1$

Case 8: $-1\langle a\langle 0$ and $-1\langle b\langle 0$

Case 9: $-1\langle a\langle 0$ and $b\langle -1$

Case 9: $a\langle -1$ and $b\langle -1$

Different types of Bifurcation diagrams are obtained for different cases of classification

6.3 Boost Converter with Parasitic Effect :

a. Mathematical Modeling.

The practical boost converter (converter with parasitic effect) circuit is shown in Fig.6.2. Switching logic of the circuit is that when switch is closed the inductor current rises and it continues till the inductor current reaches to Iref , ignoring any arriving clock pulse . As soon as the inductor current reaches to Iref , the switch is off and the inductor current falls. The switch closes again on the arrival of the next clock pulse, which is explained by the fig.5.5. A delay of δT is introduced in control logic to realize the industrial trend of higher and higher frequency as generated propagation delay in control circuit is significant for higher frequency. The circuit has two states depending on whether the control switch is opened or closed. When switch is closed (on period) the state equations are

$$L\frac{di}{dt} = V_i - ir_i$$

$$C\frac{dv_c}{dt} = -\frac{v_c}{R + r_c} \qquad \ldots\ldots\ldots \quad (6.3)$$

and the states equations during off period (when switch is off) are

$$L\frac{di}{dt} = V_i - ir_i - i\frac{Rr_c}{R + r_c} - v_c\frac{R}{R + r_c}$$

$$C\frac{dv_c}{dt} = -\frac{v_c}{R + r_c} + \mathrm{i}\frac{R}{R + r_c} \qquad \ldots\ldots\ldots \quad (6.4)$$

where Vi= constant for Pure DC and Vi = $|V_m Sin\omega t|$ for Rectified DC

We obtain the stroboscopic map under the following assumptions which have been adopted in a number of earlier studies [8], [9].

- The capacitor connected in parallel with the load is large enough so that the fluctuation in the output voltage is insignificant.
- The switching period (T) is short enough (i.e. T/RC << 1) for which the inductor current to be essentially linear during the on and off periods.

b. **Bifurcations:** In most practical converters the ripple amplitude is less than 1% of the output voltage and a high value of capacitance satisfies the second condition. This makes the above assumptions reasonable. If clock pulse period (T) is much smaller than the RC time constant the output voltage (Vo) is significantly constant. The slopes of the inductor current during on period and off period are Vi/L=m_1 and (Vo-Vi)/L=m_2 respectively where L=inductance, Vo= output voltage & Vi= input voltage of the converter. Vi= constant for Pure DC and Vi = $|V_m Sin\omega t|$ for Rectified DC . The borderline between the two cases is given by the value of I_n for which the inductor current reaches I_{ref} exactly at the arrival of the next clock pulse, i_{n+1} is the next clock current value of i_n.

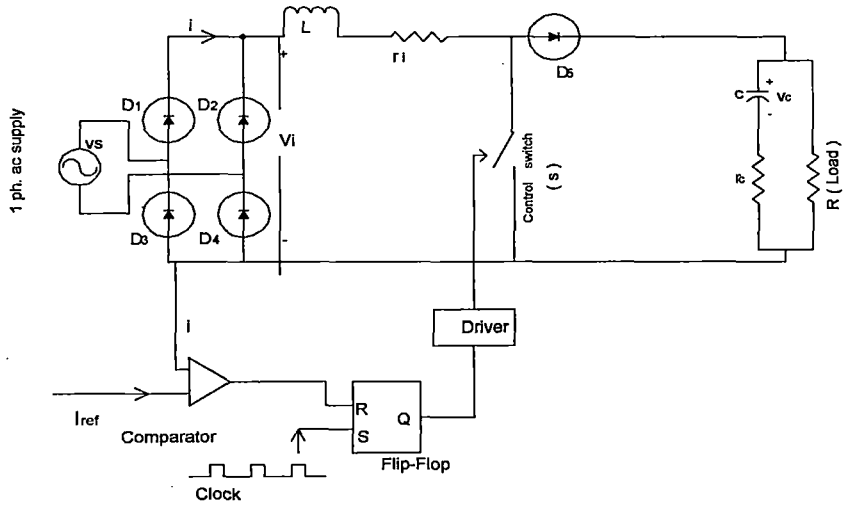

Fig. 6.2. The current mode controlled boost converter with parasitic effect and rectified DC input. For pure DC input Vi is a pure DC voltage instead of a rectifier and ac input.

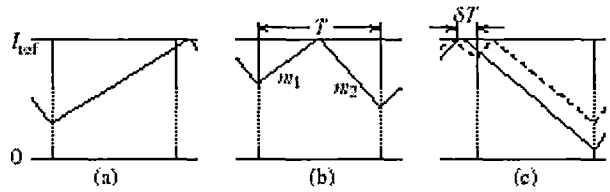

Fig. 6.3 Time plot of inductor current of the boost converter between two consecutive clock pulses the switch remains on (b) the switch remains both on and off (c) firm line indicates clock comes before δT delay of switch off and dashed line indicates clock comes after δT delay of switch off

Due to the delay of δT in the control logic, the inductor current has two borderlines I_{b1} and I_{b2} in the state space as follows:

$$I_{b1} = (V_i / R) + (I_{ref} - (V_i / R)) * e^{(R*T/L)} \quad \text{.....(6.5)}$$

$$I_{b2} = ((V_0 - V_i) / R) + (I_{ref} - ((V_0 - V_i) / R)) * e^{(R*\delta T/L)} \quad \text{.....(6.6)}$$

The map is obtained from the equations (6.3), (6.4), (6.5) and (6.6) as :

$$I_{n+1} = (V_i / R) - (I_n - (V_i / R)) * e^{(-R*T/L)} \quad \text{for } I_n \le I_{b1}$$

$$I_{n+1} = -(V_o / R) * (1 - (V_i - I_n * R)/(V_i - I_{ref} * R) * e^{(-R*T/L)}) + (V_i / R) + (I_n - (V_i / R)) * e^{(-R*T/L)}$$

$$\text{for } I_{b1} \le I_n < I_{b2}$$

$$I_{n+1} = ((V_0 - V_i) / R) - (I_n + ((V_0 - V_i) / R)) * e^{(R*T/L)} \quad \text{for } I_n > I_{b2} \quad \text{.....(6.5)}$$

where Vi= constant for Pure DC and Vi = $|V_m Sin\omega t|$ for Rectified DC

Here the map is continuous across the border I_{b1} but is discontinuous across the border I_{b2}

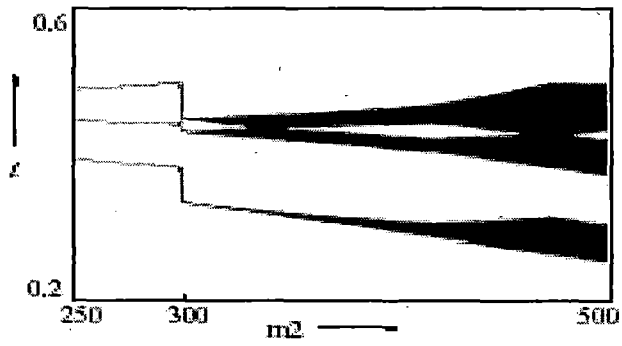

Fig. 6.4 Bifurcation diagram for the boost converter with delay in control loop for pure DC input

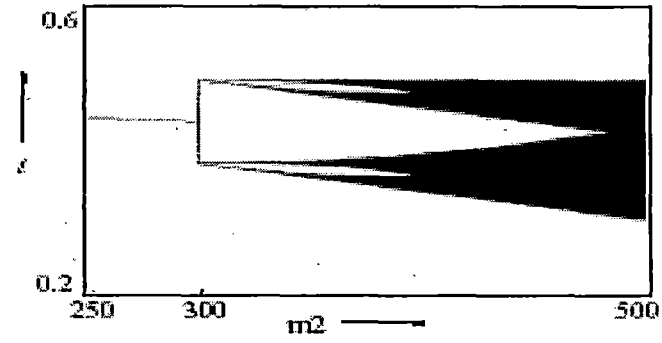

Fig. 6.5 Bifurcation diagram for the boost converter without delay in control loop for pure Dc input

The numerically obtained bifurcation diagram is shown in fig. (6.4) – (6.9). The parameter values are: Vi= 30 V, L = 0.1 H, T = 400 μ s, Vo is varied and I_{ref} = 0.5 A. Among the diagram fig. 6.4 and 6.5 are already developed in [14]. Fig. (6.6) - (6.9) are is developed using the same method as in [14] with the parasitic effect. To obtain fig. 6.6 and 6.8 input Vi is taken as pure dc voltage and fig. 6.7 and 6.9 input Vi is taken as rectified single phase voltage. We study the bifurcation in the system as a function of the parameter α = m2/m1. We find that there is a stable Period-1 orbit so long as $\alpha < 1$. This condition of stability of the Period-1 solution (duty ratio <0:5) is well known in the theory of dc–dc converters. However, as α increases through unity, there is a period doubling bifurcation. Since R_B is linear, none of the points on R_B or their higher iterates can be stable. Therefore the

fixed point moves discontinuously to the border. As the slope of R_A is unity, the resulting border collision bifurcation falls on the borderline between Cases 8 and 4. Notice that the behavior for both the regions of the parameter space is chaotic for $\mu > 0$. Thus, there is a chaotic attractor after the border collision bifurcation. As expected, there is no periodic window for further change in the parameter.The chaotic orbit is robust. This is important from a practical point of view. It has been proposed to use chaos productively in spreading the spectrum of dc–dc converters [9], [13]. In such applications it would be necessary to ensure that the system does not come out of chaos into a periodic window due to small inadvertent change of parameters. The above observation gives a clue to designing converters with no periodic windows within the chaotic range of operation.

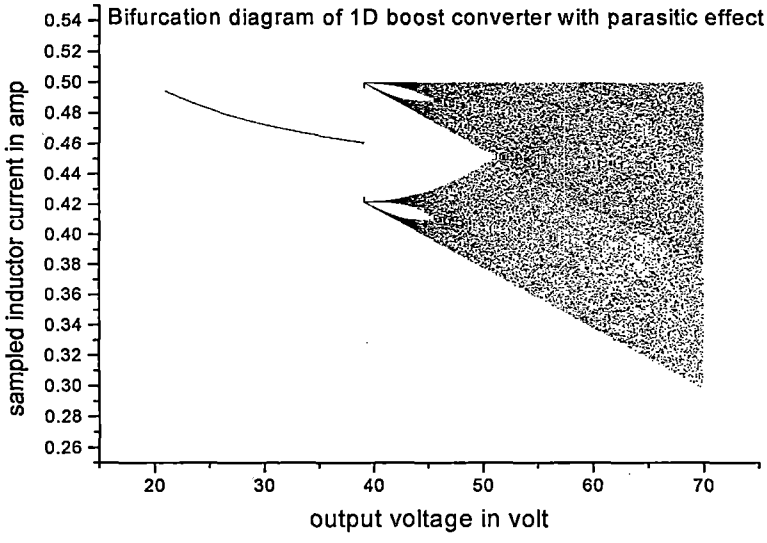

Fig.6.6. The bifurcation diagram of the current mode controlled pure DC fed boost converter with parasitic effect and without delay.

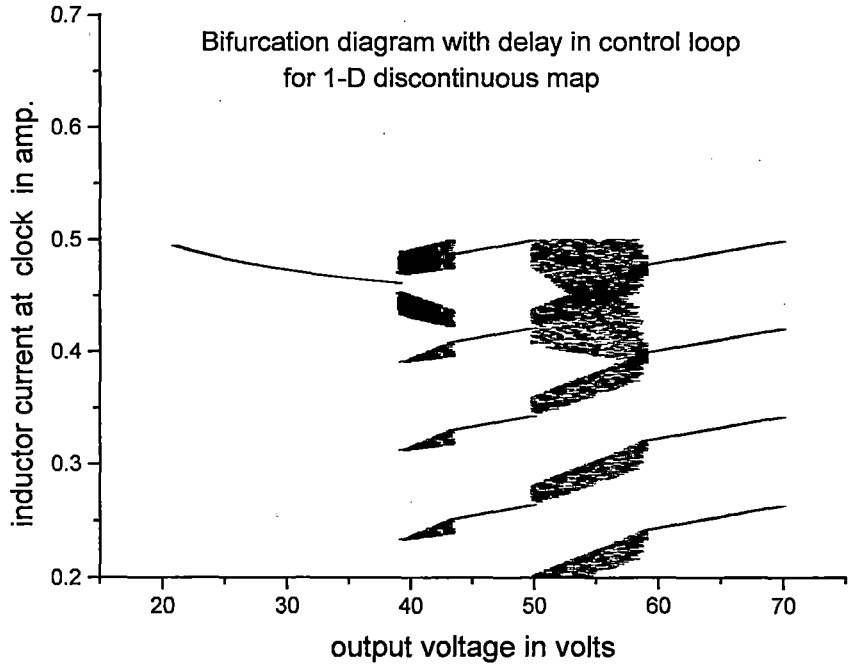

Fig.6.7. The bifurcation diagram of the current mode controlled pure DC fed boost converter with parasitic effect and with delay.

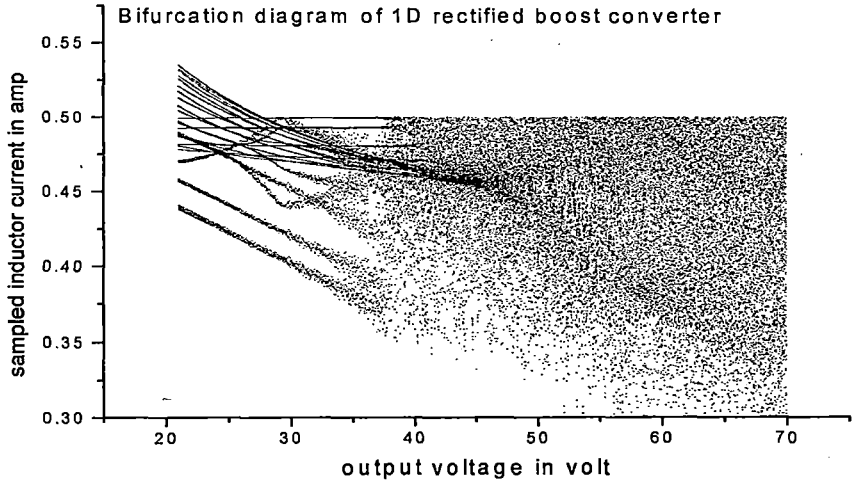

Fig.6.8. The bifurcation diagram of the current mode controlled Single phase rectified DC fed boost converter with parasitic effect and without delay.

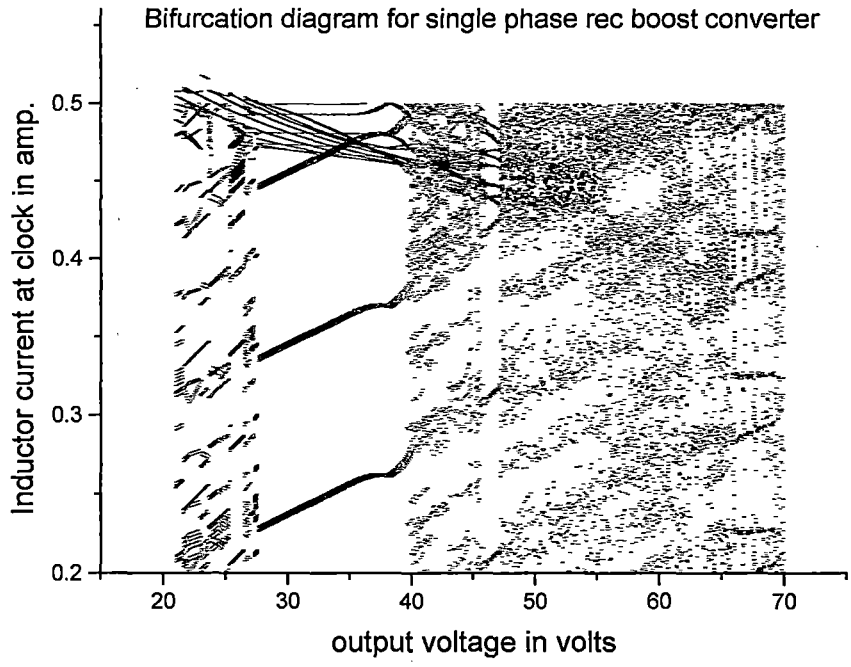

Fig.6.9. The bifurcation diagram of the current mode controlled
Single phase rectified DC fed boost converter with parasitic effect and with delay.

6.4. Conclusions:

Here we have applied the theory of bifurcations in 1-D discontinuous piecewise smooth piecewise monotonic maps. We have shown that however complicated the map of a real system may be, the border collision bifurcations can be understood only in terms of its piecewise affine approximation at the borders. We have developed the 1-D discontinuous modeling of the boost converter with parasitic effect for two types of source voltage one for pure DC & another for Rectified DC. We presented the different Bifurcations diagram for the developed 1-D discontinuous modeling which are useful in analyzing, identifying and describing the nonlinear phenomena in such circuits.

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